# EIC3600 COMMERCIAL DATABASE SEARCH REQUEST

58

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☐ RUSH - SPE signature required: _____

**Business Methods Case:** 705/26
Write in 705 subclass(es) to search required files for 705 cases or cases cross referenced in 705.

Requester's Full Name: Forest Thompson Examiner # : 76652 Date: 05/16/2003

Art Unit: 3625 Phone Number 306-5449 Serial Number: 09/579825

Bldg & Room #: 7B27 Results Format Preferred: PAPER ☐ DISK ☐ E-MAIL ☐

**If more than one search is submitted, please prioritize searches in order of need.**

**Provide the PALM Bib page or the following:**

Title of Invention: **BEHAVIORAL SYNTHESIS ELECTRONIC DESIGN AUTOMATION TOOL BUSINESS-TO-BUSINESSAPPLICATION SERVICE PROVIDER**

Inventors (provide full names): **Elof Frank; Bernd Braune; David Knapp; Hans-Joachim Schmidt**

**Earliest Priority Filing Date:** 05/26/1999

**Requested attachments:**

- If possible, provide the cover sheet, the IDS, examples, or relevant citations, authors, etc, if known.
- Please attach copies of the parts of this case that help explain or are most pertinent to this search. Examples are: ***abstract, background, summary, claim(s)*** ***[not all of the claims].***

**The claimed or apparent novelty of the invention is:**

Claim Language: A business-to-business application service provider with a software tool environment offered on a pay-per-use basis for syste-on-a-chip designers to create unique intellectual property, comprising:

An Internet website able to accepts uploads of electronic designs written in a hardware description language (HDL);

A subscription controller that provides for a billing of said system-on-a-chip designer as a condition of downloading back a simulated and verified derivative of electronic design over the Internet;

Whereas user are charged a pay-per-use to create a unique intellectual property.

**This search should focus on:**

(Also include keywords or synonyms)

**KEYWORDS:**

Software pay-per-use Internet on-line service provider electronic circuit design
Modular circuit design electronic design automation using hardware descriptive language (HDL)
Electronic design automation (EDA)

Special Instructions or Other Comments

-03 12:18 RCVD

Send to *STIC-EIC3600 (email)*

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Dr.Link _____
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WWW/Internet ✓
Other (specify) _____

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            EWARE? OR FIRMWARE?
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            ARE()DESCRIPT?
S3     417352   SUBSCRIB? OR SUBSCRIPTION OR PAY??? OR BILL? ? OR PAY(2N)(-
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            END?
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**11/5/1 (Item 1 from file: 2)**
DIALOG(R)File 2:INSPEC
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5050817 INSPEC Abstract Number: B9510-0100-081, C9510-5600-001
**Title: Proceedings International Phoenix Conference on Computers and Communications**
Publisher: IEEE, New York, NY, USA
Publication Date: 1995 Country of Publication: USA xvii+742 pp.
ISBN: 0 7803 2492 7
U.S. Copyright Clearance Center Code: 95/$4.00
Conference Title: Proceedings International Phoenix Conference on Computers and Communications
Conference Date: 28-31 March 1995 Conference Location: Scottsdale, AZ, USA
Language: English Document Type: Conference Proceedings (CP)
Abstract: The following topics were dealt with: distributed systems; multiprocessors; parallel processing; hypercubes; data **transmission** ; protocols; broadband **networks** ; Cayley graphs; the information highway; **software** management; direct graphs; object-oriented **programming** ; formal verification; **circuit design** ; parallel architectures; parallel **programming** ; performance analysis; communication **networks** ; ATM; synchronization; switching **networks** ; phase shift keying; video-on-demand and multimedia communications; mobile communications; and performance evaluation.
Subfile: B C
Descriptors: computer science; information networks; telecommunication
Identifiers: distributed systems; multiprocessors; parallel processing; information highway; graphs; communication networks; ATM; performance evaluation
Class Codes: B0100 (General electrical engineering topics); B6200 ( Telecommunication); C5600 (Data communication equipment and techniques); C5440 (Multiprocessing systems); C5470 (Performance evaluation and testing); C4230 (Switching theory); C6100 (Software techniques and systems)
Copyright 1995, IEE

**11/5/2 (Item 2 from file: 2)**
DIALOG(R)File 2:INSPEC
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4916343 INSPEC Abstract Number: B9505-0100-034, C9505-1200-003
**Title: 1993 (25th) Southeastern Symposium on System Theory**
Publisher: IEEE Computer Society Press, Los Alamitos, CA, USA
Publication Date: March 1993 Country of Publication: USA xviii+601 pp.
ISBN: 0 8186 3560 6
U.S. Copyright Clearance Center Code: 93/$3.00
Conference Title: 1993 (25th) Southeastern Symposium on System Theory
Conference Sponsor: IEEE; Univ. of Alabama, Tuscaloosa
Conference Date: 7-9 March 1993 Conference Location: Tuscaloosa, AL, USA
Language: English Document Type: Conference Proceedings (CP)
Abstract: The following topics are dealt with: electromagnetics; electric machines and power electronics; personal computers in power engineering education; power systems; electronics; optics and radar; modeling and simulation; expert systems; neural networks; control systems; system identification; robotics; fuzzy systems; neural **networks** for pattern recognition; **electronic design** automation and testing; **software**

engineering; parallel processing and **networks** ; parallel processing algorithms; signal processing; image processing; communication networks; and bandwidth-efficient **transmission** .

Subfile: B C

Descriptors: bandwidth compression; CAD; control engineering; electric machines; electromagnetic fields; electromagnetic waves; electronic engineering; electronic equipment testing; expert systems; fuzzy systems; identification; modelling; neural nets; optics; parallel processing; pattern recognition; power electronics; power engineering; radar; robots; signal processing; simulation; software engineering; system theory; telecommunication networks

Identifiers: system theory; electromagnetics; electric machines; power electronics; personal computers; power engineering education; power systems ; electronics; optics; radar; modeling; simulation; expert systems; neural networks; control systems; system identification; robotics; fuzzy systems; pattern recognition; electronic design automation; testing; software engineering; parallel processing; signal processing; image processing; communication networks; bandwidth-efficient transmission

Class Codes: B0100 (General electrical engineering topics); B5000 ( Electromagnetic fields); B8000 (Power systems and applications); B6100 ( Information and communication theory); B6200 (Telecommunication); C1200 ( Systems theory and cybernetics); C1300 (Control theory); C6100 (Software techniques and systems); C7400 (Engineering computing); C5200 (Logic design and digital techniques)

Copyright 1995, IEE

**11/5/3 (Item 3 from file: 2)**

DIALOG(R)File 2:INSPEC

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03795939 INSPEC Abstract Number: B91000692, C91012566

**Title: ECAD-status and prospects (electronics CAD)**

Author(s): Young-Uk Yu

Journal: Korea Information Science Society Review vol.8, no.3 p. 5-13

Publication Date: 1990 Country of Publication: South Korea

CODEN: CHKWEN ISSN: 1015-9908

Language: Korean Document Type: Journal Paper (JP)

Treatment: General, Review (G)

Abstract: Discusses electronic design automation; DRAMs; the trend in single-user workstation power; LANs; TCP/IP ( **transmission** control protocol/ **Internet** protocol); simulation **software** ; level sensitive scan design; LSI and VLSI; VHDL (VHSIC **hardware description** language); the behavioural, structural and physical domains; verification; bottom-up and top-down designs; layout CAD; schematic editors; ASICs; structured computer-aided logic design (SCALD); hand-crafted design; the 'rip-up and retry' method; back annotation; built-in self test; automatic test equipment; EDIF; IGES; behavioural description; and silicon compilers. (7 Refs)

Subfile: B C

Descriptors: circuit CAD; circuit layout CAD; reviews

Identifiers: behavioural domain; structural domain; physical domain; bottom up designs; electronics CAD; electronic design automation; DRAMs; single-user workstation power; LANs; TCP/IP; transmission control protocol/Internet protocol; simulation software; level sensitive scan design; LSI; VLSI; VHDL; VHSIC hardware description language; verification; top-down designs; layout CAD; schematic editors; ASICs; structured computer-aided logic design; SCALD; hand-crafted design; rip-up and retry; back annotation; built-in self test; automatic test equipment; EDIF; IGES; behavioural description; silicon compilers

Class Codes: B1130B (Computer-aided circuit analysis and design); C7410D (Electronic engineering)

**11/5/4 (Item 4 from file: 2)**
DIALOG(R)File 2:INSPEC
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03681166 INSPEC Abstract Number: B90048972, C90053714
**Title: Interconnection network simulator (INS)**
Author(s): Manighalam, S.
Author Affiliation: AT&T Bell Labs., Whippany, NJ, USA
Journal: AT&T Technical Journal vol.68, no.6 p.63-72
Publication Date: Nov.-Dec. 1989 Country of Publication: USA
CODEN: ATJOEM ISSN: 8756-2324
Language: English Document Type: Journal Paper (JP)
Treatment: Applications (A); Practical (P); Product Review (R)
Abstract: The increasing speed of today's digital systems has imposed new demands on interconnection network design. To help ensure quality designs, a way was needed to assess the performance of the interconnection network early in the design process. However, existing design systems did not support **transmission** line and circuit analyses. Now, the interconnection **network** simulator (INS)-an interactive, menu-driven simulation **program** -provides this capability. The INS allows a **circuit** designer to simulate the entire interconnection **network** under active conditions and provides graphs of the voltage, current, and frequency responses for evaluating the network's performance. Its online editing feature permits the designer to alter the electrical, geometrical, and physical parameters of the simulated network to increase its performance. The INS has been incorporated into several general computer-aided design systems, giving them the transmission line and circuit analysis capabilities that they lacked. (1 Refs)
Subfile: B C
Descriptors: circuit analysis computing; circuit CAD; digital simulation; transmission line theory
Identifiers: transmission line analysis; circuit analysis; interactive program; voltage response; AT&T; current response; frequency response; network performance; electrical parameters; geometrical parameters; digital systems; interconnection network design; interconnection network simulator; menu-driven simulation program; graphs; online editing; physical parameters ; computer-aided design systems
Class Codes: B1130B (Computer-aided circuit analysis and design); B5240 (Transmission line theory); B1150F (Distributed linear networks); C7410D ( Electronic engineering)

**11/5/5 (Item 5 from file: 2)**
DIALOG(R)File 2:INSPEC
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02144577 INSPEC Abstract Number: B83059729, C83042422
**Title: ZyP: a new design automation system based on standard cells for VLSI design**
Author(s): Loesch, W.
Author Affiliation: ZyMOS Corp., Sunnyvale, CA, USA
Conference Title: Electro/82 Conference Record p.5-3/1-5
Publisher: Electron. Conventions, El Segundo, CA, USA
Publication Date: 1982 Country of Publication: USA 1140 pp.
Conference Date: 25-27 May 1982 Conference Location: Boston, MA, USA
Language: English Document Type: Conference Paper (PA)

Treatment: New Developments (N); Practical (P)
Abstract: ZyMOS Corporation has created ZyP, a system that provides a very high level of design automation. ZyPs operation is analogous to a mathematical transform that maps parameters from one coordinate system to another: a description of logical functions is transformed into photolithographic masks. Available to **subscribing** designers, ZyP is a combination of existing CAD tools, original ZyMOS **software** , and **applications** libraries which are linked together to form a powerful, user-friendly custom **circuit design** tool. Zyp can be accessed through an international timesharing communications **network** . The ZyP design system may also be installed on a computer at the customer's facility. (0 Refs)
Subfile: B C
Descriptors: cellular arrays; circuit CAD; large scale integration; logic CAD
Identifiers: design automation system; standard cells; VLSI design; ZyMOS Corporation; logical functions; photolithographic masks; CAD tools; applications libraries; custom circuit design; timesharing communications network
Class Codes: B1130B (Computer-aided circuit analysis and design); B1265 (Digital electronics); B2550G (Lithography); B2570 (Semiconductor integrated circuits); C5210B (Computer-aided logic design); C7410D ( Electronic engineering)

**11/5/6 (Item 6 from file: 2)**
DIALOG(R)File 2:INSPEC
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00016776 INSPEC Abstract Number: B69004174, C69001874
**Title: Computer aided design of electronic circuits**
Author(s): Roska, T.
Journal: Meres es Automatika vol.16, no.7-8 p.277-83
Publication Date: 1968 Country of Publication: Hungary
CODEN: MEAUAI ISSN: 0025-9993
Language: Hungarian Document Type: Journal Paper (JP)
Abstract: Introductory paper on **application** of digital computers to **circuit design** . A generalised RLC **network** containing linear active element is analysed in terms of **transfer** function and an equivalent circuit suitable for computer analysis is generated. Methods for determination of transfer characteristic, amplitude and phase transmission, sensitivity to component tolerances is discussed in general terms. An example of an emitter follower with capacitive emitter-to-base feedback for increase of input impedance is worked out in full detail. The program for this was written for a medium size computer in Gier-Algol language. (18 Refs)
Subfile: B C
Descriptors: computer-aided circuit analysis; computer-aided circuit design; equivalent circuits; network analysis
Class Codes: B1130B (Computer-aided circuit analysis and design); C7410D (Electronic engineering)

**11/5/7 (Item 1 from file: 99)**
DIALOG(R)File 99:Wilson Appl. Sci & Tech Abs
(c) 2003 The HW Wilson Co. All rts. reserv.

2179140 H.W. WILSON RECORD NUMBER: BAST96065017
**Hands-on Internet**
Bateman, Cyril;

Electronics World v. 102 (Oct. 1996) p. 760-1
DOCUMENT TYPE: Feature Article ISSN: 0959-8332 LANGUAGE: English
RECORD STATUS: Corrected or revised record

ABSTRACT: A brief overview of mirrors, **electronics design** data, and new ways of searching old services on the **Internet** is presented. Two FTP **software download** sites catering for Windows systems, Winsite and Simtel.Net, are widely mirrored. In addition, **electronic design** data **websites** such as QuestNet, Elantec, and Electric Library provide technical support and help designers select and source semiconductors or integrated circuits worldwide. FInally, Deja News saves time by searching only within the Usenet News Groups, thereby eliminating the time consuming manual searching previously needed to locate a topic.

DESCRIPTORS: Internet--Directories;

**11/5/8 (Item 1 from file: 233)**
DIALOG(R)File 233:Internet & Personal Comp. Abs.
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00492914 98CW04-116

**IT overhaul may boost fashion profit -- Liz Claiborne swaps old systems for new in bid to get more flexible**

Vijayan, Jaikumar
Computerworld , April 13, 1998 , v32 n15 p55-56, 2 Page(s)
ISSN: 0010-4841
Company Name: Liz Claiborne
Languages: English
Document Type: Articles, News & Columns
Geographic Location: United States

Presents a look at Liz Claiborne Inc. the New York, NY-based apparel maker as it plans to replace more than 80 percent of its old computer infrastructure by next year. Cites John Sullivan, the company's vice president of information systems, who says the biggest challenge of the technology overhaul has been teaching people to cope with change. States that the company will bring on specialized package applications to run on Oracle databases. Alm all old systems have been replaced by Hewlett-Packard Co. Uni Microsoft Windows NT servers. Mentions that one application is decision support warehouse which will be rolled out companywide later this year. Says now the company used to fly in retailers to review new designs, but now **sends design** information **electronically** via the **Web** . Notes that an in-house **application** allows for trackin purchase orders instantly rather than by telephone. (bjp)

Descriptors: Corporate Information; Planning; Internet; Data Warehousing; Retailing; Corporate Reorganization
Identifiers: Liz Claiborne

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S1   19559800   APPLICATION? OR SOFTWARE? OR PROGRAM? OR FREEWARE? OR SHAR-
             EWARE? OR FIRMWARE?
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             RDWARE()DESCRIPT?
S3   13430680   SUBSCRIB? OR SUBSCRIPTION OR PAY??? OR BILL? ? OR PAY(2N)(-
             USE OR USAGE) OR CHARG??? OR BILLING
S4      48175   S1(10N)S2
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             BER? OR LAN OR WAN OR SERVER?)
S6         60   S5(10N)(S3 OR FEE OR FEES)
S7         27   S6 NOT PY>1999
S8         10   RD (unique items)
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         (c) 2003 San Jose Mercury News
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         (c) 2003 The Gale Group
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01726069 03-77059
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**Bill processing simplified by the Internet**

ABSTRACT: MSFDC, a joint venture between Microsoft Corp. and First Data Corp., has developed an Internet bill delivery and payment system that will allow customers to receive and pay customized bills over the Internet. Currently, some of the largest billers and bill processors are participating in an MSFDC pilot program. Billers using the service should reap significant cost savings. MSFDC estimates a savings of 20%-40% of the biller's current variable billing and remittance costs with the Internet bill delivery and payment (IBDP) system./To help billers connect to the MSFDC Service Center, a Systems Integrator Program has been established. IBDP's set-up eases customers fears about Internet security.

Wipf, Kara
Water Engineering & Management v145n11 PP: 30-32 Nov 1998 CODEN: WENMD2
ISSN: 0273-2238 JRNL CODE: WEM
DOC TYPE: Journal article LANGUAGE: English LENGTH: 3 Pages
WORD COUNT: 2225

**8/7/2 (Item 2 from file: 15)**
DIALOG(R)File 15:ABI/Inform(R)
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01354613 00-05600
**USE FORMAT 9 FOR FULL TEXT**
**EDA vendors discover Internet**

ABSTRACT: Electronic-design-automation vendors moved quickly to embrace the Internet in 1996. Announcements this year showed that the Internet is rapidly becoming a mechanism for distributing and supporting EDA software, providing models and implementing component-information and design-management systems.

Goering, Richard
Electronic Engineering Times n933 PP: 48, 66 Dec 23, 1996 ISSN: 0192-1541 JRNL CODE: ELET
DOC TYPE: Journal article LANGUAGE: English LENGTH: 2 Pages
WORD COUNT: 1433

**8/7/3 (Item 1 from file: 16)**
DIALOG(R)File 16:Gale Group PROMT(R)
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06873574 Supplier Number: 58248451 (THIS IS THE FULLTEXT)
**Sun Microsystems, Lucent, Synopsys, and Avnet Team with Internet Startup, Toolwire, To Deliver New Approach for B2B Engineering Collaboration. (Company Business and Marketing)**
EDGE: Work-Group Computing Report, pNA
Dec 13, 1999
TEXT:
Toolwire Tuesday announced that it has teamed with Sun Microsystems, Lucent, Synopsys and Avnet to deliver powerful software design tools, top-of-the-line hardware servers, and virtually unlimited access to

high-performance computing resources to engineers, from anywhere, anytime and on demand. For the first time, engineers and businesses can " **pay** -per-**use** " to leverage a premiere suite of **electronic design** automation ( **EDA** ) tools and productivity services through a **web** -based **application** service provider (ASP) workbench at **www** .toolwire.com.

Toolwire, along with its partners, redefines the current computing paradigm by making state-of-the-art engineering technology and related engineering services accessible via the desktop browser, without the up-front multi-million dollar hardware and software investments currently required. This alliance with Toolwire also represents a very aggressive B2B strategy by technology leaders -- Sun, Lucent, Synopsys and Avnet -- to enable distributed engineering teams and partnering companies to collaborate on the next generation of electronic products destined for the home, the business and powering the Internet itself.

"Toolwire has the future of computing services well defined," said Sun Microsystems' Fred James, EDA Relations Manager. "Their web-based ASP approach is where we see the future of not only EDA tools but many strategic software packages in general." As a member of Sun's Incubator Program, Toolwire will leverage industrial-strength Sun hardware and software technologies to scale to any engineer or engineering team's computing requirements. Sun is also helping Toolwire to ensure instant 24x7 access at a security level that matches or exceeds that available on in-house networks.

"Previously, companies would have to spend millions of dollars and months of time and effort setting up and maintaining these design software tools and other computing resources that Toolwire has made available on-demand," said Dan Hodges, CEO and founder of Toolwire. "No other vendor has attempted to make such sophisticated, heavy-duty and powerful design software available through an ASP format like Toolwire has done together with its partners. Toolwire essentially levels the playing field for companies designing next generation technology or consumer products, bringing corporations to new levels of cost efficiency and effectiveness."

A New Design Environment that Will Significantly Impact the Industry

Two strong forces are everyday realities of today's electronics industry -- next generation consumer and business products are requiring more complex technology, and increased market competition is challenging electronics manufacturers to race their products to market faster than ever before. Time-to-market execution is a business imperative for all companies wishing to succeed in the new millennium. Electronic design is one of the most important, yet time-consuming, stages of product development for popular consumer items like the Palm Pilot, every day appliances like the PC, and the hardware fabric of the Internet itself that allows us to buy groceries online.

The software and hardware required to run the in-house electronic design operations for products like these come at a great price -- the EDA industry exceeds $3 billion annually and the associated infrastructure costs are greater than $8 billion. Productivity enhancing advances in this industry enable companies to conceive, design and launch new products faster, to better compete for a larger portion of the overall multi-trillion dollar electronics product market.

Toolwire, with its partners, dramatically simplifies the product development process by aggregating familiar tools and services onto a web-accessed workbench. Toolwire allows the design infrastructure to be fully outsourced while providing much greater utility and flexibility. Toolwire gives vendors, like Sun, Lucent, Synopsys and Avnet, an excellent platform on which to deliver their tools and provides designers with broad access to the widest possible range of resources. It also gives partnering businesses an easy way to collaborate on joint product designs in a B2B capacity.

Industry Leaders Align with Toolwire

Lucent's programmable logic customers are being directed to Toolwire

for instant, online access to the ORCA Foundry design tool. "Toolwire not only gives our potential customers the ability to try our tools and devices using nothing more complicated than a web browser, but it also enables our customers to start designing silicon products now," said Fred Koons, FPGA software product planning manager at Lucent's Microelectronics Group.

Synopsys is working with Toolwire to provide access to FPGA Express, its widely used synthesis tool. "Toolwire services are standards-based, familiar, and available to anyone with Internet access," said Jay Michlin, vice president and general manager of FPGA products at Synopsys. "Ultimately, Toolwire seeks to bring to Synopsys the advantages that make the Internet so popular in so many other business areas."

Toolwire has partnered with Avnet Design Services to provide the technical support and design services essential to every product's development. In addition, the Toolwire Workbench will provide fast links to additional Avnet services.

"The power of the distributed engineering desktop created by Toolwire has unleashed the full potential of the Internet and created the first collaborative design environment to span multiple companies and resource communities," said Warren Miller, vice president of Strategic Marketing and Business Development for Avnet Design Services. "This Toolwire vision of the future of EDA supports the delivery of a comprehensive web of tools, knowledge and services now required by design engineers. They do it by pushing the desktop into a distributed environment and to the exact applications and computing performance needed for each phase of design. We expect the design productivity gains to dramatically improve our customers' time-to-market."

Phoenix, Arizona-based Avnet, Inc., a Fortune 500 company with annual sales exceeding $6.35 billion, is one of the world's largest distributors of semiconductors, interconnect, passive and electromechanical components and computer products from leading manufacturers. Serving customers in 59 countries, Avnet markets, inventories and adds value to these products and provides world-class supply-chain integration, engineering design and technical services. The company's Web site is located at www.avnet.com.

Since its inception in 1982, a singular vision -- The Network Is The Computer -- has propelled Sun Microsystems, Inc., to its position as a leading provider of industrial-strength hardware, software and services that power the Internet and allow companies worldwide to ".com" their businesses. With $12.4 billion in annual revenues, Sun can be found in more than 170 countries and on the World Wide Web at http://www.sun.com.

Lucent Technologies designs, builds and delivers a wide range of public and private networks, communications systems and software, data networking systems, business telephone systems and microelectronics components. Bell Laboratories is the research and development arm of the company. For more information about Lucent Technologies, visit its Web site at http://www.lucent.com.

Synopsys Inc., is the leading supplier of electronic design automation (EDA) products and services to the global electronic market. The company provides comprehensive design technologies to creators of advanced integrated circuits, electronic systems and systems on a chip. Synopsys also provides consulting services and support to its customers to streamline the overall design process and accelerate time-to-market. Additional information about Synopsys is available at http://www.synopsys.com.

Toolwire is a comprehensive application service provider (ASP) delivering web-based EDA tools and productivity services to the electronic design industry. Toolwire users realize dramatically reduced upfront costs and greater productivity by leveraging a web-based infrastructure. Toolwire enables vendor partners to extend their service levels and broaden their market reach. A standard web browser is used to access complete design flows linking multiple tools or to operate a specific point tool as an extension of the designer's local desktop. Toolwire owns and maintains the

servers on which these applications are run, ensuring instant access to tools and services at a security level that matches or exceeds that available on in-house. More information on the company and its products can be found at www.Toolwire.com, by calling 408/980.5881, or by email at info@Toolwire.com. Toolwire's investors include Artemis Ventures (www.artemisventures.com), Angel Investors LP (www.svangel.com) and Barrington Partners (www.barringtonpartners.com).

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05752008 Supplier Number: 50235812 (THIS IS THE FULLTEXT)

**Actel Announces Availability of Second Device in High-Performance Family of FPGAs; New SX Addition Features 4ns Clock-To-Out and 320MHz Maximum Clock Rate.**

Business Wire, p08100149
August 10, 1998
TEXT:

SUNNYVALE, Calif.--(BUSINESS WIRE)--Aug. 10, 1998--Actel Corp. (NASDAQ:ACTL) today announced the newest device in its fastest family of field programmable gate arrays (FPGAs), the 32,000-gate A54SX32.

The SX family features 4ns clock-to-out speeds and 320MHz maximum clock rates enabling high-performance FPGA solutions for applications from gigabit Ethernet to 66MHz, fully-compliant PCI designs.

With a combination of high performance and high capacity, the A54SX32 enables designers to integrate multiple high-performance complex programmable logic devices (CPLDs) into a single FPGA, cutting power consumption, saving board space and reducing cost. The A54SX32 is well suited for use in networking, telecommunications, data acquisition, instrumentation, medical electronics and high-speed computer peripheral applications. This is the second device in Actel's new SX family and follows the 16,000-gate A54SX16 announced earlier this year.

"The SX family was designed with one thing in mind -- to provide designers with a high performance FPGA that enables them to easily achieve their performance goals. This ease of speed solution enables the designer to achieve shorter design cycles and get to market quicker," said Deon Spicer, product line manager, Actel Corp. "The A54SX32 offers ASIC-like performance, which allows designers to work in leading edge applications."

The high performance of the SX family is achieved by several innovative architectural features including a hard-wired clock (320MHz maximum clock frequency), fast I/O's (4ns Clock-to-Out), abundant local interconnects (direct connect 0.1ns, fast connect 0.4ns) and a new low-impedance metal-to-metal antifuse. This combination permits the SX family to exceed the performance of CPLD's; for example, SX devices can perform a 32-bit wide decode function in 7.7ns pin-to-pin.

Additional SX Family Features

The SX FPGA family has been designed to give customers maximum performance, enabling leading-edge data communications applications such as 8b/10b encoding for gigabit Ethernet routers, high-speed interfacing for DS3 networks and fully-compliant, 66MHz PCI designs.

The SX device family offers clock-to-out speeds of 4ns and input setup times under 0.6ns. All SX devices have full pin compatibility within the family and provide mixed 5/3.3-volt support with 3.3-volt output drive and 5-volt tolerant inputs.

Design and Debug Tools

The ability to achieve full device utilization is a significant benefit to designers of programmable logic devices, allowing them to reduce

die area, cost and design time. The Actel Designer software provides 100-percent automatic place and route capability reaching up to 100-percent utilization of SX devices. Easy debug capabilities will be offered using Actel's Silicon Explorer, a computer-based debugging and diagnostic tool suite for real-time in-system design, debug and verification activities.

Actel's Designer Lite full-function development tools are available free of **charge** . Customers can register for the **software** on Actel's **Web** site at **www** .actel.com. **EDA** support for SX is provided by the following Actel partners: Cadence, Exemplar Logic, Mentor Graphics, Model Technology, Synopsys/Viewlogic and Synplicity.

Availability and Packaging

Samples of the A54SX32 are available now. Actel will offer a wide selection of popular packages including PQFP208, PLCC84, TQFP176, PGBA313, EBGA329, CQFP208 and CQFP256.

About Actel

Actel is dedicated to providing logic designers with the capability and confidence to successfully move up to higher complexity designs. The company is the world's leading supplier of antifuse-based field programmable gate arrays (FPGAs) and associated software development tools. FPGAs are used by designers of communications, computer, medical, military/aerospace, industrial control, and other electronic systems to differentiate their products and get them to market faster. Actel is traded on the Nasdaq National Market under the symbol ACTL and is located at 955 East Arques Avenue, Sunnyvale, California, 94086-4533. Telephone: 408/739-1010. Internet: http://www.actel.com.

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04817243 Supplier Number: 47087943 (THIS IS THE FULLTEXT)
**American Companies in Japan: COMPUTERS AND PERIPHERALS**
Japan-U.S. Business Report, v1997, n329, pN/A
Feb 1, 1997
TEXT:
In January the Cray Research subsidiary of SILICON GRAPHICS INC. installed at Kyoto UniversityUs Institute for Chemical Research a Cray T94 vector supercomputer and a Cray Origin2000 supercomputing server as well as two SGI PowerChallenge supercomputing servers and an Onyx InfinteReality graphics supercomputer. The T94 system replaces a Cray Y-MP2E supercomputer. It has four ultra high-speed microprocessors and 1 gigabyte of main memory. ICRUs Origin2000 server is the high-end model, which scales

128 MIPS R1000 64-bit RISC (reduced instruction-set computing) processors and has a main memory of 16 gigabytes. Each of the PowerChallenge supercomputer servers has 32 processors; one has 4 gigabytes of internal memory, while the other has double that. The four-processor Onyx graphics system features 2 gigabytes of main memory. This hardware allows ICR to perform traditional supercomputing in computational chemistry, parallel data processing and mining in biological data bases. It also gives the research organization real-time visualization capabilities. ICR is

using the system for such computer-intensive research experiments as creating and analyzing data bases related to the Human Genome Project, an international effort to decipher the entire internal structure of human DNA (deoxyribonucleic acid).

The Tokyo-based subsidiary of UNISYS CORP. has delivered to OITA BANK, LTD. the first of a new generation of financial sector-oriented TRITON systems. The Oita, Oita prefecture-based bank is using the system, which consists of four 2200/5422 servers operating in parallel, for round-the-clock on-line transactions processing. HYAKUGO BANK, LTD. of Tsu, Mie prefecture and KIYO BANK, LTD. of Wakayama, Wakayama prefecture worked with the Unisys affiliate in developing the TRITON package.

New from DATA GENERAL CORP.Us Japanese operation is the first Windows NT clustering solution packaged as a single rack-mounted system. The NT Cluster-in-a-Box is based on two AViiON servers, each of which can run up to four 200-megahertz Pentium Pro processors with 512 kilobytes of integrated cache memory per processor and up to 4 gigabytes of external memory. It comes with a fault-tolerant CLARiiON disk-array storage system, plus Data GeneralUs NTAlert automated problem detection service support and Firstwatch for NT failover software from VERITAS SOFTWARE CORP. of Mountain View, California. A standard configuration of the NT Cluster-in-a-Box is priced around $170,000. It is being targeted for applications where data integrity and high availability are priorities.

HEWLETT-PACKARD JAPAN LTD. has put on the market four aggressively priced entry-level models in the HP 9000 D-class Enterprise Server family. The D220 and the D320 systems are powered by a single 132-megahertz PA-7300LC PA-RISC processor, while the D230 and the D330 systems feature a 160-megahertz PA-7300LC chip. The base configuration of each model includes 128 kilobytes of primary cache, 32 megabytes of internal memory and 2 gigabytes of disk memory. The four servers offer a price/performance improvement of up to 50 percent over their D-class predecessors as well as expanded Internet functionality. HP Japan will supply the new products to HITACHI, LTD. and NEC CORP. on an OEM basis.

Meanwhile, HEWLETT-PACKARD JAPAN LTD. added to the HP NetServer Series the low-cost LD Pro line, which is targeted at the requirements of small and midsize workgroups and remote sites. The lineUs two models are priced between $5,100 and $6,300. That street price provides Pentium Pro processing, a super-fast Ultra SCSI (small computer system interface) port, an EDO (extended data-out) memory subsystem and a preinstalled high-speed network interface card as well as high availability features. Sales of the HP NetServer LD Pro are projected at 5,000 units in the first year on the market. .....HEWLETT-PACKARD JAPAN LTD. has cut the prices of the midrange HP NetServer LH Series by anywhere from 16.2 percent to 36 percent. Now, for example, the LH Pro6/200SMP Model 1 costs $9,500, more than a third less than before.

The local subsidiary of SUN MICROSYSTEMS INC. claimed a price/performance breakthrough in introducing the latest addition to the SPARCstation 5 line of workstations. With a list price starting at $9,400, the Model 170 provides twice the processing power of its predecessor at a 30 percent price savings. That price includes 32 megabytes of internal memory, 2.1 gigabytes of disk storage, a 17-inch color monitor, TurboGX graphics and Solaris Internet Access PlusPack software. Sun **bills** the Model 170 as ideal for such uses as **software** development, including **Internet** and **intranet applications , electronic design** automation

and mechanical computer-aided design drafting systems.

Around midyear Nampa, Idaho-based MICRON ELECTRONICS, INC., which opened a subsidiary in Chiba, Chiba prefecture last fall (see Japan-U.S. Business Report No.J326, November 1996, p.J10), plans a major marketing push in the corporate sector for its Windows NT/Pentium Pro-equipped machines. Affiliates of MI-TSUI & CO., LTD. and NISSHO IWAI CORP. are in charge of corporate sales, while ADO ELECTRONIC INDUSTRIAL CO., LTD. is handling retail sales through its T-Zone stores. These channels are expected to produce 90 percent of Micron ElectronicsU sales, with the balance coming from catalog orders. In three years the company hopes to have between 3 percent and 5 percent of the Japanese PC market. To help reach this goal the subsidiary expects this year to triple its technical support and engineering staff to 150 people.

Nine foreign-affiliated and Japanese PC suppliers unveiled machines in January built around INTEL CORP.Us new Pentium MMX microprocessor. Short for multimedia extension, the Pentium MMX chip processes video images, sound and other multimedia information as much as 60 percent faster than a standard Pentium processor, making it a plus for such applications as teleconferencing and running DVD software. Among the companies introducing PCs equipped with a Pentium MMX, which is available in speeds of 150, 166 and 200 megahertz, were: DELL COMPUTER CORP., DIGITAL EQUIPMENT CORP., GATEWAY 2000 INC., IBM JAPAN LTD. and PACKARD BELL NEC INC. Similar machines were announced by HITACHI, LTD., SANYO ELECTRIC CO., LTD., SEIKO EPSON CORP. and TOSHIBA CORP. However, Japan PC market leaders NEC CORP. and FUJITSU, LTD. opted to wait to avoid undercutting prices on their current machines.

New on the market is the ChemBook 9750-S20 notebook PC from CHEM USA CORP. Running off a 200-megahertz Pentium processor, the Hayward, California-based firmUs powerful system provides 48 megabytes of EDO internal memory, 2.1 gigabytes of disk storage, a 1.44-megabyte floppy disk drive and an 8X CD-ROM drive. It also has a 13.3-inch active-matrix liquid crystal display screen. Distributor TAKITA RESEARCH & DEVELOPMENT CO., LTD. has priced the standard configuration at $5,000. It expects to sell 3,000 units in the first year through mail order.

Start-up AUGMENT SYSTEMS, INC. of Westford, Massachusetts has tapped MARUBENI ELECTRONICS CO., LTD. as the exclusive distributor of its high-end Macintosh super server. The AFX 410 is designed to reduce the time required to access, move and process large data files in the publishing and printing industries. Accessed through the Mac desktop, the system transfers files to and from the server at rates of 10 megabytes per second or more using a 1-gigabit-per-second-bandwidth fibre channel arbitrated loop. It offers up to 100 gigabytes of disk storage and automatic tape backup and archiving.

Working with AVAL DATA CORP. of Atsugi, Kanagawa prefecture, DIGITAL EQUIPMENT CORP.Us subsidiary has developed two versions of a server that calls back a personal computer connected to an in-house local area network. That feature prevents unauthorized access to a companyUs system from outside as well as facilitates secure money transfers. The CSG-1040, which can handle four telephone lines simultaneously, is priced at $1,400. The CSG-1080, with double the capacity, lists for $1,700. Aval Data expects to sell 3,000 of each model in the first year of marketing.

Through its subsidiary EMC CORP. has introduced a product that combines its Symmetrix storage system technology with a real-time operating system, thereby providing high-performance and high-capacity storage and delivery of multimedia applications over high-speed networks. The Symmetrix Network Media Storage system can be connected directly to a LAN. With different software, the SNMS can do double-duty as a file server.

IBM JAPAN LTD. is marketing the Network Printer series of high-speed laser printers for LANs. The lineUs three products range in price from $1,600 to $3,900. Depending on the model, they can print either 11.5, 16 or 24 A4-size pages a minute. With an optional card installed, the printers also can work in mixed network environments.

HEWLETT-PACKARD CO. is revamping its local market strategy for ink-jet printers. To date the company has supplied printers for Windows-based machines on an OEM basis to NEC CORP., while HEWLETT-PACKARD JAPAN LTD. has specialized in marketing printers for Macintosh machines. Now HP and NEC are in the process of codeveloping printers for the Windows market that will be sold under each partnerUs brand name. Their first product, a color system, is due to go on sale in March.

An exchange rate of Y118=$1.00 was used in this report.

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04749657 Supplier Number: 46991219 (THIS IS THE FULLTEXT)

**EDA vendors discover Internet**

Electronic Engineering Times, p48
Dec 23, 1996

TEXT:

Electronic-design-automation vendors moved quickly to embrace the Internet in 1996. Announcements this year showed that the Internet is rapidly becoming a mechanism for distributing and supporting EDA software, providing models and implementing component-information and design-management systems.

Today, virtually every EDA vendor has a World Wide Web page. While some are little more than glorified brochures, others provide models, free software or useful information about bugs and workarounds.

Designers who used to call vendors or mail requests for information are now finding what they need within a few minutes of surfing the Web.

Internet newsgroups such as comp.cad.vhdl, comp.cad.synthesis and sci.electronics.cad carry on lively debates about such topics as Linux vs. Windows NT, hardware keys and EDA software quality. Independent forums like the E-Mail Synopsys Users Group (jcooley@world.std.com) provide hands-on information from users about EDA software problems and issues.

The Internet may be a boon to small, niche EDA companies that don't want to build a sales force. Epsilon Design Systems (Milpitas, Calif.), an FPGA synthesis startup, hopes to leverage the Internet as a distribution arm so the company can plow up to 50 percent of revenues back into research, said Steve Lin, vice president of technology.

This year, however, was just the initial wave of what may become a much larger trend. Research at the University of California at Berkeley suggests that EDA software may someday be provided on a pay-per-access basis over the Internet, and that Java could even be a next-generation design language.

Though it's impossible to predict all the ways the Internet will affect EDA in years to come, one thing is becoming increasingly clear: The business models upon which the EDA industry is built may have to dramatically change as a result.

The ability to download and even purchase EDA software from the Internet was evident by 1996 announcements. For instance, MathSoft Inc. (Cambridge, Mass.) opened its WebStore, which offers a range of applications including the company's flagship Mathcad product (www.mathsoft.com). Users can test products before purchasing them, use the CheckFree credit-card information service to **pay** for the **software** and then automatically download it.

Even more ambitious is **EDA** Mall, a **Web** site now under construction by value-added-reseller NuCAD Systems (Colorado Springs, Colo.). Jeff Thayer, NuCAD president, outlined several features that will be included at this site.

First is an on-line index of some 400 vendors, including anyone "even remotely related" to EDA, Thayer said. Then, vendors will be invited to set up "virtual stores" through which users can view demos and possibly download software.

Shopping tour

Finally, users will be able to buy some products online with their credit cards. Though the grand opening isn't expected until February, the site is open for informational "tours" (www.edamall.com/).

Another way of accessing a broad variety of EDA vendor information comes from Xilinx Inc. (San Jose, Calif.), which this year launched its SmartSearch service (www.xilinx.com). SmartSearch indexes sites that are rich in programmable-logic content, and will conduct keyword searches that look through Web sites of EDA software developers, trade publications, electronics distributors, design consultants and industry organizations.

Users can construct "agent profiles" that periodically search defined Web areas for new information. For example, an agent could be created to monitor all EDA development sites for new information on synthesis tools. In addition to the Xilinx home page, SmartSearch buttons are located on Web sites from EE Times, Cadence Design Systems, Mentor Graphics, OrCAD, Synario Design Automation and Synopsys.

Free EDA software is always an appealing prospect, and a number of 1996 Internet announcements came with the words "at no charge." In a recent example, Motorola Inc. (Phoenix) announced a free PC-based version of its Motorola Programmable Array design software (design-NET.com/fpga), which supports the MPA1016 and MPA1036 FPGA devices. Despite a very small presence in the FPGA marketplace, the Motorola site is receiving an average of two to three downloads daily, a spokesperson said.

Earlier this year, Hyperlynx placed a free graphical I/O Buffer Information Specification (IBIS) model editor at its Web site (www.hyperlynx.com). R-Active Concepts (Cupertino, Calif.) placed a visual state-chart tutorial on its Web site (www.r-active.com). And Aldec Corp. (Henderson, Nev.) is offering free versions of its state-machine and HDL editors through Jan. 31, 1997 (www.aldec.com).

Design kits

It isn't just low-end software that's appearing at Web sites without charge. Compass Design Automation (San Jose) has been offering free front-end design kits for its 0.35-micron Passport IC libraries (www.compass-da.com). The full physical libraries start at $350,000, so Passport isn't a high-volume item. Still, Compass claims that an average of 20 customers per week download the 0.35-micron design kits.

"In the past, we had to go through a time-consuming sales cycle to access design kits for the purpose of benchmarking the density and performance of our designs," said Compass customer Nabil Takla, president of Innovative Semiconductors (Mountain View, Calif.). "Compass has eliminated this bottleneck by delivering the design kits via the Web, enabling us to have instant access to reliable, industry-standard libraries."

If users can preview, purchase and download EDA software from the Web, the next question that emerges is support. Few EDA companies have been as active in this area as Synopsys Inc. (Mountain View, Calif.), which this year announced its 1 millionth transaction on Solv-It!, the company's Web-based customer-support system (www.synopsys.com).

Solv-It! is an online knowledge database containing answers to common questions in the form of articles. A "transaction" is defined as the actual download of an article rather than a hit on the site.

Zuken-Redac (Santa Clara, Calif.) customers on maintenance have access to the Program for Internet Information Exchange (PIIE), which provides an interactive customer-service information system including access to documents, hot-line support and data on bugs and workarounds (www.redac.co.uk). Users can also download software patches from PIIE. This fall, Zuken-Redac announced it was making PIIE available through e-mail as

well (majordomo@redac.co.uk).

User forums such as the E-Mail Synopsys User's Group (ESNUG) provide another avenue of support. That forum was launched by EDA "consumer activist" John Cooley over Synopsys' original opposition, but today, Synopsys engineers are frequent contributors.

Meanwhile, Accel Technologies (San Diego) offers two unmoderated, uncensored user groups, one for P-CAD users (pcadusers@acceltech.com) and one for Accel EDA users (eda users@acceltech.com).

Closely related to the dissemination of EDA tools and services over the Net is the availability of models. One of the most interesting developments in this area is a largely unpublicized effort from Mentor Graphics Corp. (Wilsonville, Ore.) called eParts (www.eparts.com).

This site opened in 1995 with a selection of product news, demonstrations and searchable catalogs. It is now evolving into a "storefront," where users can purchase off-the-shelf simulation models and symbol libraries, as well as custom-built parts. Products now available include digital- simulation models from Mentor's Board Process Library and symbol elements produced by Mentor's Axiom symbol compiler.

Mentor is now deploying a plan in which users will submit a purchase order through a Mentor Graphics account manager, pick up a "shopping cart," search catalogs, and purchase and download the parts.

Viewlogic Systems Inc. (Marlboro, Mass.) this year set up Modelsite, a location where users can browse lists of Viewlogic and third-party models (www.viewlogic.com). An engineer can enter a bill of materials and the type of model needed, and initiate a search. Models are included for schematic capture, simulation, timing analysis, pc-board floor planning and signal integrity. Mike O'Reilly, director of systems marketing at Viewlogic, said the site had received 16,000 hits from its March 15 opening through late November. At this point, he noted, Modelsite just tells customers if a model is available; next year, Viewlogic hopes to allow users to download the models.

Free Spice models, software modeling utilities and Spice reference materials are available from Intusoft (San Pedro, Calif.), which opened a Web site this year (www.intusoft.com). OrCAD (Beaverton, Ore.) announced last summer the availability of schematic symbols for Intel flash-memory components at its Web site (www.orcad.com).

The Free Model Foundation, an ad hoc organization launched by EDA users in 1995, continues to offer free VHDL models, and recently announced the addition of Intel flash-memory components. The models are unencrypted and available in VHDL source code (www.vhdl.org/vi/fmf).

Managing component data has always been a challenge, so it's no surprise that providers are taking advantage of both the Internet and corporate intranets to facilitate this task. This year Aspect Development Inc. (Mountain View) launched two Internet-related products: Aspect Online and Explore-Catalog (www.aspectdv.com). Aspect Online is a Web-based subscription service for Aspect's VIP family of reference databases. Explore-Catalog is search-and-classification software that lets customers publish catalogs on the Web.

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03339642 Supplier Number: 44621659 (THIS IS THE FULLTEXT)

**SYNOPSYS JOINS RASSP; WILL RENT SOFTWARE**

Electronic News (1991), p44
April 25, 1994

TEXT:
MOUNTAIN VIEW, CALIF. - Synopsis will participate in the Advanced Research Projects Agency's Rapid Prototyping of Application-Specific Signal Processors (RASSP) program, supplying design tools to the team led by Lockheed Sanders and becoming involved in the team's plan to offer software on a rental basis over the Internet.

ARPA last August funded two teams under the four-year RASSP program, targeted at developing a design flow and methodology for electronic systems. The Lockheed Sanders team received $42.5 million, while a Martin Marietta team got $55 million. Both teams will use VHDL in their projects.

Lockheed Sanders' team includes Motorola's Government Systems & Technology Group, Hughes Aircraft and ISX Corp., a small contractor specializing in knowledge-based, rule-based and expert systems.

Synopsys will loan its high-level design tools for ASIC designs to the Lockheed RASSP team members for non-production, proof-of-concept electronic design. The team will also purchase consulting services from Synopsys to define the methodology and process flow.

'Lockheed Sanders, Motorola, Hughes, ISX and Synopsis share the mission to find new and innovative ways to increase designers' productivity said Aart de Geus, Synopsys' president and CEO. 'In RASSP, we see another avenue to achieve this mission.'

In a fairly new wrinkle for electronic design automation, the Lockheed RASSP team will also develop a fee-for-use approach to integrating and distributing design tools over electronic networks, rather than the traditional method of licensing software on disks or CD-ROMs.

**Bill** Hood, Lockheed Sanders' RASSP **program** manager, said the idea of renting **EDA** tools over the **Internet** represents the 'Blockbuster Video approach to design tools.' In this way, companies that want to utilize tools for a short period can 'rent' software licenses through the international computer network, instead of paying the usual licensing fees for a year's use or longer.

This approach should appeal to military contractors who may want to add tool capacity at a critical period in a project, but don't want to take on the considerable expense of buying more licenses, Mr. Hood said.

The RASSP team members have collectively formed a company called Electronic Information Corp. (EIC), which will make the tools available on the Internet. Security procedures will be built in to ensure software can't be copied off the network by unauthorized users, according to Mr. Hood.

The RASSP team has approached 68 tool vendors about participating in the program as 'an alternative method of distribution,' Mr. Hood said, and Synopsys is the first to commit to it. Some 30 other tools are expected to be available at the end of May.

Many tool vendors have at least provided 'inputs' on how to run the software rental program, Mr. Hood said. 'It's been an educational process,' he added.

Rita Glover, senior analyst for In-Stat Inc., pronounced the software rental concept 'a very interesting idea,' while stressing there are a number of issues to work out in practical implementation. 'I do think it's a viable thing to do,' she said.

One question is 'how to deal with the learning curve, without documentation for support,' Ms. Glover said. If the users are already familiar with the tool they are renting, then that issue becomes less critical. 'Some major (tool) vendors have started offering on-line documentation,' she added, but that can't always substitute for on-site hand-holding.

The In-Stat analyst said she was 'dubious that some tool vendors would want to get into it,' especially manufacturers of programmable logic devices who want to bind their customers to proprietary software.

A spokesman for Cadence Design Systems said, 'We are working with the Lockheed Sanders team to help define the environment in which they're going to do the design,' especially in the area of digital signal processor

design. 'We are delivering technology to them,' he added.

Regarding EIC and its Internet-based rental program, the Cadence spokesman said the concept had 'some potential,' but was 'not our primary focus' with the RASSP program. Cadence has declined, at this point, to commit to the EIC offerings.

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08590129 SUPPLIER NUMBER: 18182581 (THIS IS THE FULL TEXT)

**DAC will target end-users this year. (Design and Automation Conference) (Industry Trend or Event)**

Bradley, Gale
Electronic News (1991), v42, n2111, p44(1)
April 8, 1996

TEXT:

Las Vegas--With a new plan to bring in the end-users of design software as well as the developers and marketers, the 33rd Design Automation Conference is ready to roll here from June 3-9.

This year's general chair, Thomas P. Pennino of Bell Labs, talked last week of what DAC attendees can expect that's new in June. For early arrivers, a day-long women's workshop will be held on Sunday, June 2. For electronic design automation (EDA) users, Mr. Pennino says he and the executive committee developed several "tracks" in each day's program so designers and engineers can find their forum for feedback and information.

Mr. Pennino said look for the eternal "value proposition" (getting more money for EDA work accomplished) question to be addressed, though the official title of the executive forum from 10:30 a.m.-12:00 noon on Tuesday, June 4, will be "The EDA Year in Review: CEOs, the Press and Users" at the Hilton pavilion.

The compensation question may be addressed, Mr. Pennino said, in the sessions during DAC that look at new electronic delivery or "borrowing" of **EDA** products, particularly **charging** by the time **software** was accessed over a **network** . Keynote speakers James Clark of Netscape Communications (Wednesday, June 5) and Eric Schmidt of Sun Microsystems (Thursday, June 6) may provide some insight to the viability of these "usage-sensitive" models, Mr. Pennino said.

What Mr. Pennino termed the "Microsoft model" of a low-cost initial software package that a customer "keeps paying for year after year" is not as attractive as the usage-sensitive, "telephone company-type" model, he said.

Another topic not on the formal agenda that Mr. Pennino expects to hear about in June: teamings like the recent Cadence Design Systems and Mentor Graphics pact (EN, April 1), which allows employees of each company to use the other's tools at customer sites. "With the growth of the service business, such teamings are a necessity," he said, "There can't be any more of this 'your consultant cannot use my tools' because out in the field, on site, customers don't want to hear it."

Of 378 papers submitted, 141 have been chosen for presentation at DAC, Mr. Pennino said. He noted three papers set for delivery were written in Japan and pertain to design directly for consumer products, like multimedia. "The Japanese really are the kings of consumer product design, so we expect there to be particular interest in those presentations," Mr. Pennino said.

Other topics for presentation noted were what designers need to know about formal verification methods; hardware/software co-design from both

ends (developer and user); and low-power design considerations will be covered in several sessions.

On the formal verification front, Mr. Pennino noted that not only Chrysalis Symbolic Design, but also Abstract Hardware Ltd. of the U.K., have formal verification tools ready for the market. He said to watch for coming formal method news from Israel and Nuremberg, Germany.

In the DAC advance program available currently, the schedule grid shows shading where customers and designers would have particular interest and none over the traditional DAC--EDA industry--topics, Mr. Pennino said. He noted there will be no reduction in the program for traditional DAC attendees.

Mr. Pennino said DAC is expecting more than last year's 15,000 attendees, quite a few more than the roughly 130 attendees of the first DAC in 1963, when all EDA was in-house and CAD systems were first being developed.

DAC founder P.O. Pistilli and his wife, Marie Pistilli, are managing the conference through their Boulder, Colo., firm, MP Associates. The toll-free number for information only is (800) 321-4573.

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**8/7/9 (Item 1 from file: 20)**

DIALOG(R)File 20:Dialog Global Reporter
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01427511 (THIS IS THE FULLTEXT)

**Actel Debuts Industry's Highest Performance FPGA; New SX Family Features 4ns Clock-to-Out and 320MHz Maximum Clock Rate**

BUSINESS WIRE
April 20, 1998 10:2

SUNNYVALE, Calif.--(BUSINESS WIRE)--April 20, 1998--Actel Corp. (NASDAQ:ACTL) today has set new standards for performance with the introduction of the industry's fastest family of Field Programmable Gate Arrays (FPGAs). The new SX family features 4ns clock-to-out speeds and 320MHz maximum clock rates enabling FPGA applications from Gigabit Ethernet to 66MHz, fully compliant, PCI designs. The SX family's unprecedented combination of performance and capacity enables designers to combine multiple high performance Complex Programmable Logic Devices (CPLDs) into a single FPGA, cutting power consumption, saving board space, and reducing costs. With 2ns - 25 bit internal decode and fast datapath capability, the SX architecture is the first programmable family to combine PLD and FPGA design solutions. Further, these new FPGA performance standards will dramatically reduce the time to market for designs that traditionally required high-speed gate arrays. The 16,000-gate A54SX16 device is available immediately for sampling, with the 32,000 gate A54SX32 and the 8,000 gate A54SX08 both expected in the third quarter. Device capacities for the entire family are expected to cover from 8,000 to 64,000 gates. "The advantages of the SX FPGA family go far beyond performance. The real benefit is the ease with which designers harness that speed and the leading-edge applications this device family enables," said Carl Burrow, vice president of marketing, Actel Corp. Device Applications

The SX FPGA family has been designed to give customers maximum performance, enabling leading edge data communications applications such as 8B/10B encoding for Gigabit Ethernet routers, high-speed interfacing for DS3 networks and 66MHz, fully compliant, PCI designs. "I was given the challenge of designing a PCI device which will run at both 50MHz and 25MHz as well as both 3.3V and 5V PCI signaling environments, using a programmable device in a 100-pin PQFP or smaller package," said Jason Kei, HW engineer, Cisco Systems. "Actel helped me succeed by providing me with the best solution that fulfils all functional, timing, electrical and

package requirements with their latest SX family." The SX device family offers clock-to-out speeds of 4ns and input setup times under 0.6ns, all without the need for complex phase-locked loops. The intrinsic speed of the SX device family simplifies the overall design cycle, increasing ease-of-use and improving design cycle time: -- The family's performance makes it significantly easier for
designers to manage board-level interfacing with other
components. -- Designs can achieve higher levels of performance without
resorting to complicated performance enhancing design techniques,
such as the use of redundant logic to reduce fan-out on critical
nets, or the instantiation of macros in HDL code. -- "DirectTime" timing driven place and route lets designers get the
most benefit from the devices' high speed interconnect, by
automatically placing logic functions in critical paths close
together.

The SX devices have full pin compatibility within the family and provide mixed 5/3.3-volt support with 3.3-volt output drive and 5-volt tolerant inputs. Device Architecture

The SX family is built on a 0.35-micron process using a Sea of Modules (SoM) architecture, which uses triple-layer metal to ensure a small die size.

The high performance of the SX family is enabled by the combination of the minimal die size, the Sea of Modules architecture itself, the low impedance of Actel's new metal-to-metal antifuse, and also by several innovative architectural features. These features include extremely fast local routing resources which allow the SX devices to perform up to 25-bit wide decodes in 2ns. Design and Debug Tools

Actel will support the SX family through its Designer Series FPGA development software which is optimized to save design and layout time. Together, these factors help simplify the design cycle, further reducing time-to-market and cost.

The Actel Designer software provides 100 percent automatic place and route capability at up to 100 percent utilization for the SX devices. Easy debug capabilities are offered using Actel's Silicon Explorer, a computer-based debugging and diagnostic tool suite for real-time in-system design, debug and verification activities.

Actel's Designer Lite full-function development tools are available free of **charge** . Customers can register for the **software** on Actel's **Web** site at **www** .actel.com. **EDA** support for SX is provided by the following list of Actel partners: Cadence, Exemplar Logic, Mentor Graphics, Model Technology, Synopsys, Synplicity, Veribest and Viewlogic.

"Actel's SX family is breaking new ground in the high performance FPGA market," said Andrew Haines, vice president of marketing, Synplicity Inc. "Performance applications will be well served by the inherent speed of SX devices coupled with the excellent quality of results that can be achieved through our Synplify FPGA synthesis tool." Pricing and Availability

The SX family includes four devices with capacities of 8,000, 16,000, 32,000, and 64,000 gates, in commercial, industrial and military temperature ranges. Device availability and pricing is as follows:

Max.
High Vol. Availa- Device Gates I/O Packages
Price bility
- -- - A54SX08 8,000 125 PQFP208, PLCC84, TQFP176, $ 8.90 3Q98
VQFP100 A54SX16 16,000 175 PQFP208, PQFP240, PLCC84, $ 15.50 NOW
VQFP100, TQFP176, EBGA329,
CQFP208, CQFP256 A54SX32 32,000 245 PQFP208, PQFP240, PLCC84, $ 27.00 3Q98
TQFP176, PBGA313, EBGA329
CQFP208, CQFP256 A54SX64 64,000 340 PQFP208, PQFP240, TQFP176, $ 55.00 1Q99

EBGA329, CQFP256

The SX Family is available for purchase directly from Actel Corp. or through the following distributors: Arrow Electronics, Pioneer-Standard Electronics, and Wyle Electronics. "We are pleased to offer Actel's SX Family to our customers. The device provides superior speed and performance as well as ease of use," said Michael Rohleder, president and CEO of Wyle Electronics. "Our customers are sure to benefit from this new device family." About Actel

Actel is dedicated to providing logic designers with the capability and confidence to successfully move up to higher complexity designs. The company is the world's leading supplier of antifuse-based field programmable gate arrays (FPGAs) and associated software development tools. FPGAs are used by designers of communications, computer, medical, military/aerospace, industrial control, and other electronic systems to differentiate their products and get them to market faster. Actel is traded on the NASDAQ National Market under the symbol ACTL and is located at 955 East Arques Avenue, Sunnyvale, Calif. 94086-4533. Telephone: 408/739-1010. Internet: http:

Copyright 1998 Business Wire. Source: World Reporter (Trade Mark).

**8/7/10 (Item 1 from file: 635)**

DIALOG(R)File 635:Business Dateline(R)
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1036489 00-00947

**Moving the money**

Glanz, William

Baltimore Business Journal (Baltimore, MD, US), V16 N38 p13
PUBL DATE: 990205
WORD COUNT: 1,017
DATELINE: Baltimore, MD, US, South Atlantic

TEXT:

Headnote:

Business-to-business electronic commerce becomes a major force

During this year's holiday shopping season, electronic commerce took center stage as millions of consumers discovered online retailers such as bookseller Amazon.com Inc.

But when it comes to dollar volume, Internet retailing is dwarfed by business-tobusiness electronic commerce -- businesses selling goods and services online to other businesses.

About $48 billion changed hands electronically between businesses last year, according to Cambridge, Mass.-based Forrester Research.

By contrast, Internet shoppers spent just $3.4 billion in November and December, according to a survey by New York-based Jupiter Communications Co. and Green wich, Conn.-based NFO Interactive. And don't expect online retailing to eclipse business-to-business electronic commerce anytime soon. Analysts say the growth in what's become known as "electronic B-to-B" doesn't show signs of slowing down.

"You're definitely going to see growth on the business-to-business side, even though all you hear is talk about the business-toconsumer side with companies like Amazon.com," said Pawan Malhotra, senior analyst at Baltimore-based Legg Mason Wood Walker Inc.

Businesses have shared information electronically since the 1960s, using a method called electronic data interchange. Creation of the Internet and developments in software and technology helped business commerce move beyond electronic data interchange and create a mammoth commercial network that thrives, even though it gets little attention.

Forrester estimates transactions through business-to-business electronic commerce will grow to $109 billion this year and $1.3 trillion by 2003 as more industries begin revising procurement methods and buy on the World Wide Web.

Despite the rosy financial outlook, there are technology challenges ahead. While Internet retailing is usually a straightforward transaction that takes place between one buyer and one seller over a product with a fixed price, business-to-business electronic commerce can be a logistical nightmare.

"In a business-to-business model there is more complexity," said Liz Sara, vice president of market ing at Rockvillebased Space Works Inc., which develops softvare that wholesalers use in their effort to market products online to other businesses.

Electronic commerce software developers such as Space Works must account for the fact that buying and selling among businesses must take place in real time, because deadlines are more crucial than during retail purchases. In addition, prices aren't necessarily the same for all purchasers in a business-to-business transaction. Delivery **charges** and terms for payment can vary.

Most companies developing **electroniccommerce** solutions **design** **Internet** -based **software** , sell the **software** to a client and install it on the client's own network.

Less common in the industry is an ecommerce method that also includes Web hosting.

Hunt Valley-based CyberSystem Technologies Inc. is one of the key players in that niche. CyberSystem -- founded in 1996 by Brian R Stauffer with the help of private equity capital from Baltimore-based venture capital company Anthem Capital LP and $250,000 from the Maryland Department of Business and Economic Development -- focuses on businesses in the health, research and pharmaceutical industries that want to develop online procurement

CyberSystem develops and operates online procurement websites for companies interested in buying products. CyberSystem came up with the term "IntraMall" to describe its approach. The malls operate on a client's intranet- an in-house Internet - but CyberSvstem hosts the site on its own server.

CyberSystem president George P. Dreyer said the hosted method of business-to-business e-commerce works best, because non-hosted technology means the software must run an online commerce program on a client's computer network.

That adds technology and maintenance issues that most businesses do not have the expertise or time to deal with, Dreyer said;

"We couldn't have done this five years ago, because the network wasn't in place. Now, everyone has an Internet connection," Dreyer said.

Bode Akintola 21-May-03

'This works because Web browsers are ubiquitous."

CyberSystem is hoping to make a name for itself with its National Institutes of Health IntraMall, its first major project. CyberSystem launched the IntraMall in August 1997 when it installed the first online-buying program at the National Cancer Institute.

By June 1998, the NIH IntraMall was open for use at all 24 NIH centers and institutes. CyberSystem is under contract to operate the IntraMall through July 2001.

The site lists products from 100 vendors, and 1,325 NIH employees have authorization to buy products through the site. It is compared to a supplies catalog. The big difference between a paper catalog and an online catalog site is convenience. An employee can order materials immediately.

A key element of the software is its ability to do all the appropriate accounting so that purchases are recorded and subtracted from a company's budget.

The NIH buys about $1.2 billion in lab supplies and equipment each year. In 1997, 96.7 percent of all NIH transactions were under $2,500, with an average cost of $400 per order. The site is intended for purchases of less than $100,000.

No matter what niche they fit into, electronic-commerce solution providers are expecting their markets to grow as more businesses embrace online buying and selling with suppliers, purchasers and their corporate partners.

"Corporate America has been moving rapidly toward this the past few months," Sara said.

Space Works employs 60 people and plans to add about 20 workers this year to accommodate an expected increase in business.

CyberSystem expects to more than double its work force from 20 to 46 people by the end of 1999. CyberSystem also expects to exceed its 1998 estimated revenue of $3.3 million.

So far, technology and financial services companies are the biggest users of business-to-business electronic commerce. Revenue generated through business-to-business transactions will grow enormously when the manufacturing sector endorses the online method, Malhotra said.

"The biggest issue for business-to-business is when does the manufacturing sector jump on the bandwagon?" Malhotra said.

"When they do, a lot of the need for wholesalers in the middle is cut out" Use of business-to-business e-commerce could cause consumer prices to fall, said David Alschuler, vice president of Bostonbased information-technology research and marketing firm Aberdeen Group, because business-to-business electronic commerce lowers costs and increases a company's efficiency.

"It means that companies that master electronic commerce have the opportunity to lower costs to the consumer," Alschuler said.

(Photograph Omitted)

Captioned as: CyberSystem Technologies Inc. president George P Dreyer

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**8/3,K/1 (Item 1 from file: 15)**
DIALOG(R)File 15:ABI/Inform(R)
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01726069 03-77059
**Bill processing simplified by the Internet**
Wipf, Kara
Water Engineering & Management v145n11 PP: 30-32 Nov 1998
ISSN: 0273-2238 JRNL CODE: WEM
WORD COUNT: 2225

...TEXT: in online bill payment of more than 80 percent per year.

Pilot partners are installing **software** , recruiting pilot customers, testing connectivity to MSFDC, **designing electronic bills** and service **Web** sites, and establishing operating procedures. All biller pilot partners receive a free biller pilot kit...

**8/3,K/2 (Item 2 from file: 15)**
DIALOG(R)File 15:ABI/Inform(R)
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01354613 00-05600
**EDA vendors discover Internet**
Goering, Richard
Electronic Engineering Times n933 PP: 48, 66 Dec 23, 1996
ISSN: 0192-1541 JRNL CODE: ELET
WORD COUNT: 1433

...TEXT: com). Users can test products before purchasing them, use the CheckFree creditcard information service to **pay** for the **software** and then automatically download it.

Even more ambitious is **EDA** Mall, a **Web** site now under construction by value-added-reseller NuCAD Systems (Colorado Springs, Colo.). Jeff Thayer ...

**8/3,K/3 (Item 1 from file: 16)**
DIALOG(R)File 16:Gale Group PROMT(R)
(c) 2003 The Gale Group. All rts. reserv.

06873574 Supplier Number: 58248451 (USE FORMAT 7 FOR FULLTEXT)
**Sun Microsystems, Lucent, Synopsys, and Avnet Team with Internet Startup, Toolwire, To Deliver New Approach for B2B Engineering Collaboration.(Company Business and Marketing)**
EDGE: Work-Group Computing Report, pNA
Dec 13, 1999
Language: English Record Type: Fulltext
Document Type: Newsletter; Trade
Word Count: 1290

(USE FORMAT 7 FOR FULLTEXT)
TEXT:
...engineers, from anywhere, anytime and on demand. For the first time, engineers and businesses can " **pay** -per- **use** " to leverage a premiere suite of **electronic design** automation ( **EDA** ) tools and productivity services through a **web** -based **application** service provider (ASP) workbench at **www** .toolwire.com.

**8/3,K/4 (Item 2 from file: 16)**
DIALOG(R)File 16:Gale Group PROMT(R)
(c) 2003 The Gale Group. All rts. reserv.

05752008 Supplier Number: 50235812 (USE FORMAT 7 FOR FULLTEXT)
**Actel Announces Availability of Second Device in High-Performance Family of FPGAs; New SX Addition Features 4ns Clock-To-Out and 320MHz Maximum Clock Rate.**
Business Wire, p08100149
August 10, 1998
Language: English Record Type: Fulltext
Article Type: Article
Document Type: Newswire; Trade
Word Count: 670

... and verification activities.
Actel's Designer Lite full-function development tools are available free of **charge** . Customers can register for the **software** on Actel's **Web** site at **www** .actel.com. **EDA** support for SX is provided by the following Actel partners: Cadence, Exemplar Logic, Mentor Graphics...

**8/3,K/5 (Item 3 from file: 16)**
DIALOG(R)File 16:Gale Group PROMT(R)
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04817243 Supplier Number: 47087943 (USE FORMAT 7 FOR FULLTEXT)
**American Companies in Japan: COMPUTERS AND PERIPHERALS**
Japan-U.S. Business Report, v1997, n329, pN/A
Feb 1, 1997
Language: English Record Type: Fulltext
Document Type: Newsletter; Trade
Word Count: 1477

... storage, a 17-inch color monitor, TurboGX graphics and Solaris Internet Access PlusPack software. Sun **bills** the Model 170 as ideal for such uses as **software** development, including **Internet** and **intranet applications** , **electronic design** automation and mechanical computer-aided design drafting systems.
Around midyear Nampa, Idaho-based MICRON ELECTRONICS...

**8/3,K/6 (Item 4 from file: 16)**
DIALOG(R)File 16:Gale Group PROMT(R)
(c) 2003 The Gale Group. All rts. reserv.

04749657 Supplier Number: 46991219 (USE FORMAT 7 FOR FULLTEXT)
**EDA vendors discover Internet**
Electronic Engineering Times, p48
Dec 23, 1996
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 1480

... Users can test products before purchasing them, use the CheckFree credit-card information service to **pay** for the **software** and then automatically download it.
Even more ambitious is **EDA** Mall, a **Web** site now under construction

by value-added-reseller NuCAD Systems (Colorado Springs, Colo.). Jeff Thayer...

**8/3,K/7 (Item 5 from file: 16)**
DIALOG(R)File 16:Gale Group PROMT(R)
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03339642 Supplier Number: 44621659 (USE FORMAT 7 FOR FULLTEXT)
**SYNOPSYS JOINS RASSP; WILL RENT SOFTWARE**
Electronic News (1991), p44
April 25, 1994
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 655

... electronic networks, rather than the traditional method of licensing software on disks or CD-ROMs.
**Bill** Hood, Lockheed Sanders' RASSP **program** manager, said the idea of renting **EDA** tools over the **Internet** represents the 'Blockbuster Video approach to design tools.' In this way, companies that want to...

**8/3,K/8 (Item 1 from file: 148)**
DIALOG(R)File 148:Gale Group Trade & Industry DB
(c)2003 The Gale Group. All rts. reserv.

08590129 SUPPLIER NUMBER: 18182581 (USE FORMAT 7 OR 9 FOR FULL TEXT)
**DAC will target end-users this year. (Design and Automation Conference) (Industry Trend or Event)**
Bradley, Gale
Electronic News (1991), v42, n2111, p44(1)
April 8, 1996
ISSN: 1061-6624 LANGUAGE: English RECORD TYPE: Fulltext; Abstract
WORD COUNT: 639 LINE COUNT: 00052

... said, in the sessions during DAC that look at new electronic delivery or "borrowing" of **EDA** products, particularly **charging** by the time **software** was accessed over a **network** . Keynote speakers James Clark of Netscape Communications (Wednesday, June 5) and Eric Schmidt of Sun...

**8/3,K/9 (Item 1 from file: 20)**
DIALOG(R)File 20:Dialog Global Reporter
(c) 2003 The Dialog Corp. All rts. reserv.

01427511 (USE FORMAT 7 OR 9 FOR FULLTEXT)
**Actel Debuts Industry's Highest Performance FPGA; New SX Family Features 4ns Clock-to-Out and 320MHz Maximum Clock Rate**
BUSINESS WIRE
April 20, 1998 10:2
JOURNAL CODE: WBWE LANGUAGE: English RECORD TYPE: FULLTEXT
WORD COUNT: 920

(USE FORMAT 7 OR 9 FOR FULLTEXT)

... and verification activities.
Actel's Designer Lite full-function development tools are available free of **charge** . Customers can register for the **software** on Actel's **Web** site at **www** .actel.com. **EDA** support for SX is provided by the following

list of Actel partners: Cadence, Exemplar Logic...

**8/3,K/10 (Item 1 from file: 635)**
DIALOG(R)File 635:Business Dateline(R)
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1036489 00-00947
**Moving the money**
Glanz, William
Baltimore Business Journal (Baltimore, MD, US), V16 N38 p13
PUBL DATE: 990205
WORD COUNT: 1,017
DATELINE: Baltimore, MD, US, South Atlantic

TEXT:

...aren't necessarily the same for all purchasers in a business-to-business transaction. Delivery **charges** and terms for payment can vary.

Most companies developing **electroniccommerce** solutions **design** **Internet** -based **software** , sell the **software** to a client and install it on the client's own network.

Less common in...

```
Set     Items   Description
S1    2029763   APPLICATION? OR SOFTWARE? OR PROGRAM? OR FREEWARE? OR SHAR-
               EWARE? OR FIRMWARE?
S2      20981   EDA OR (ELECTRONIC? OR CIRCUIT)(1N)DESIGN? OR HDL OR HARDW-
               ARE()DESCRIPT?
S3      73189   SUBSCRIB? OR SUBSCRIPTION OR PAY??? OR BILL? ? OR PAY(2N)(-
               USE OR USAGE)
S4     876546   UPLOAD? OR DOWNLOAD? OR TRANSFER? OR TRANSMI? OR SENT OR S-
               END?
S5     330448   ONLINE OR ON()LINE OR INTERNET OR INTRANET OR WEB? OR HOME-
               PAGE OR HOME()PAGE OR NETWORK? OR PORTAL? OR WWW OR CYBER? OR
               LAN OR WAN OR SERVER?
S6       1897   S1(10N)S2
S7         96   S6(10N)S5
S8        966   S2(10N)S4
S9         10   S8(20N)S3
S10        30   S7(S)(S3 OR S4)
S11        25   (S10 OR S9) AND IC=G06?
? show file
File 348:EUROPEAN PATENTS 1978-2003/Apr W04
         (c) 2003 European Patent Office
File 349:PCT FULLTEXT 1979-2002/UB=20030515,UT=20030508
         (c) 2003 WIPO/Univentio
```

**11/3,K/1 (Item 1 from file: 348)**
DIALOG(R)File 348:EUROPEAN PATENTS
(c) 2003 European Patent Office. All rts. reserv.

01444845
**Embedded logic analyser**
**Eingebetteter logischer Analysator**
**Analyseur logique integre**
PATENT ASSIGNEE:
Altera Corporation, (398574), 101 Innovation Drive, San Jose, California 95134, (US), (Applicant designated States: all)
INVENTOR:
Veenstra, Kerry, 1906 Conifer Court, San Jose, California 95132, (US)
Rangasayee,Krishna, 2350 Meadowlake Drive, Pleasanton, CA 94566, (US)
Herrmann, Alan L., 727 Winstead Terrace, Sunnyvale, California 94087, (US)
LEGAL REPRESENTATIVE:
O'Connell, David Christopher (62551), Haseltine Lake & Co., Imperial House, 15-19 Kingsway, London WC2B 6UD, (GB)
PATENT (CC, No, Kind, Date): EP 1233341 A1 020821 (Basic)
APPLICATION (CC, No, Date): EP 2002009367 981118;
PRIORITY (CC, No, Date): US 65602 P 971118; US 186607 981106
DESIGNATED STATES: DE; FR; GB; IT; NL
RELATED PARENT NUMBER(S) - PN (AN):
EP 919916 (EP 98309432)
INTERNATIONAL PATENT CLASS: **G06F-011/25** ; G01R-031/3177; G01R-031/3185
ABSTRACT WORD COUNT: 255
NOTE:
Figure number on first page: 5

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

| Available Text | Language | Update | Word Count |
|---|---|---|---|
| CLAIMS A | (English) | 200234 | 682 |
| SPEC A | (English) | 200234 | 17651 |
| Total word count - document A | | | 18333 |
| Total word count - document B | | | 0 |
| Total word count - documents A + B | | | 18333 |

INTERNATIONAL PATENT CLASS: **G06F-011/25** ...

...SPECIFICATION a system or in a programming station. In operation, any number of engineers use computer **network** 12 in order to develop programming instructions using an **electronic design** automation **software** tool. Once a design has been developed and entered by the engineers, the design is compiled and verified before being **downloaded** to the programming unit. The programming unit 14 is then able to use the **downloaded** design in order to program PLD 16.
For the purposes of debugging a PLD according...

**11/3,K/2 (Item 2 from file: 348)**
DIALOG(R)File 348:EUROPEAN PATENTS
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01406657
**CIRCUIT DESIGN SUPPORT METHOD AND CIRCUIT DESIGN SUPPORT SYSTEM AND PROGRAM RECORDING MEDIUM**
**SCHALTUNGSENTWURFSUNTERSTUTZUNGSVERFAHREN UND SCHALTUNGSENTWURFSUNTERSTUTZUNGSSYSTEM UND PROGRAMMAUFZEICHNUNGSMEDIUM**

**PROCEDE ET SYSTEME D'ASSISTANCE A LA CONCEPTION D'UN CIRCUIT INTEGRE**

PATENT ASSIGNEE:
Toshiba Tec Kabushiki Kaisha, (2633500), 1-1, Kanda Nishiki-cho, Chiyoda-ku, Tokyo, 101-8442, (JP), (Applicant designated States: all)
INVENTOR:
USAMI, Yutaka, 71-1, Tachibana 3-chome, Ohitocho, Tagata-gun, Shizuoka 410-2303, (JP)
LEGAL REPRESENTATIVE:
Fuchs Mehler Weiss & Fritzsche (100496), Patentanwalte Postfach 46 60, 65036 Wiesbaden, (DE)

PATENT (CC, No, Kind, Date): EP 1302877 A1 030416 (Basic)
WO 2002007015 020124
APPLICATION (CC, No, Date): EP 2001947993 010712; WO 2001JP6060 010712
PRIORITY (CC, No, Date): JP 2000219250 000719; JP 2001202453 010703
DESIGNATED STATES: DE; FR; GB
EXTENDED DESIGNATED STATES: AL; LT; LV; MK; RO; SI
INTERNATIONAL PATENT CLASS: **G06F-017/50** ; **G06F-017/60**
ABSTRACT WORD COUNT: 91
NOTE:
Figure number on first page: 0001

LANGUAGE (Publication,Procedural,Application): English; English; Japanese
FULLTEXT AVAILABILITY:

| Available Text | Language | Update | Word Count |
|---|---|---|---|
| CLAIMS A | (English) | 200316 | 1640 |
| SPEC A | (English) | 200316 | 4639 |
| Total word count - document A | | | 6279 |
| Total word count - document B | | | 0 |
| Total word count - documents A + B | | | 6279 |

INTERNATIONAL PATENT CLASS: **G06F-017/50** ...

... **G06F-017/60**

...SPECIFICATION invention relates to a circuit design support method and circuit design support system in a **server** system using a **network** , and a **program** recording medium and, more particularly, to a **circuit design** support method and circuit design support system in a **server** system which receives, through a network, circuit simulation request information **transmitted** from a client terminal and executes a circuit simulation on the basis of the request...

...result of determination whether the result of executed simulations has satisfied the specifications, and a **program** recording medium.

Disclosure of Invention

In a **circuit design** support method of the present invention, a **server** system receives, through a network, circuit simulation request information **transmitted** from a client terminal and executes a circuit simulation on the basis of the request...

...designating parameters of the circuit module, and display information that allows inputting circuit specification are **transmitted** to the client terminal. The server system receives the circuit modules selected in the client...

...of the determination are stored into a storage section. The results of the simulation are **transmitted** to the client terminal when the client terminal has access to the server system.

In...

**11/3,K/3 (Item 3 from file: 348)**
DIALOG(R)File 348:EUROPEAN PATENTS
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01034790
**Embedded logic analyzer**
**Eingebetter Logikanalysator**
**Analyseur logique imbrique**
PATENT ASSIGNEE:
Altera Corporation, (398574), 101 Innovation Drive, San Jose, California 95134, (US), (Applicant designated States: all)
INVENTOR:
Veenstra, Kerry, 1906 Conifer Court, San Jose, California 95132, (US)
Rangasayee, Krishna, 1291 Vincente Drive, #242, Sunnyvale, California 94086, (US)
Herrmann, Alan L., 727 Winstead Terrace, Sunnyvale, california 94087, (US)
LEGAL REPRESENTATIVE:
O'Connell, David Christopher et al (62551), Haseltine Lake & Co., Imperial House, 15-19 Kingsway, London WC2B 6UD, (GB)
PATENT (CC, No, Kind, Date): EP 919916 A2 990602 (Basic)
EP 919916 A3 000112
APPLICATION (CC, No, Date): EP 98309432 981118;
PRIORITY (CC, No, Date): US 65602 P 971118; US 186607 P 981105
DESIGNATED STATES: DE; FR; GB; IT; NL
EXTENDED DESIGNATED STATES: AL; LT; LV; MK; RO; SI
RELATED DIVISIONAL NUMBER(S) - PN (AN):
(EP 2002009367)
INTERNATIONAL PATENT CLASS: **G06F-011/25** ; G01R-031/3177; G01R-031/3185
ABSTRACT WORD COUNT: 255
NOTE:
Figure number on first page: 5

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

| Available Text | Language | Update | Word Count |
|---|---|---|---|
| CLAIMS A | (English) | 9922 | 1737 |
| SPEC A | (English) | 9922 | 17654 |
| Total word count - document A | | | 19391 |
| Total word count - document B | | | 0 |
| Total word count - documents A + B | | | 19391 |

INTERNATIONAL PATENT CLASS: **G06F-011/25** ...

...SPECIFICATION a system or in a programming station. In operation, any number of engineers use computer **network** 12 in order to develop programming instructions using an **electronic design** automation **software** tool. Once a design has been developed and entered by the engineers, the design is compiled and verified before being **downloaded** to the programming unit. The programming unit 14 is then able to use the **downloaded** design in order to program PLD 16.
For the purposes of debugging a PLD according...

**11/3,K/4 (Item 4 from file: 348)**
DIALOG(R)File 348:EUROPEAN PATENTS
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01030324
**MOBILE ELECTRONIC COMMERCE SYSTEM**
**MOBILES ELEKTRONISCHES HANDELSSYSTEM**
**SYSTEME DE COMMERCE ELECTRONIQUE MOBILE**
PATENT ASSIGNEE:
MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD, (216884), 1006, Oaza-Kadoma, Kadoma-shi, Osaka 571-0000, (JP), (Applicant designated States: all)
INVENTOR:
TAKAYAMA, Hisashi, 21-22, Matsubara 4-chome, Setagaya-ku, Tokyo 156-0043, (JP)
LEGAL REPRESENTATIVE:
Casalonga, Axel (14511), BUREAU D.A. CASALONGA - JOSSE Morassistrasse 8, 80469 Munchen, (DE)
PATENT (CC, No, Kind, Date): EP 950968 A1 991020 (Basic)
WO 9909502 990225
APPLICATION (CC, No, Date): EP 98937807 980813; WO 98JP3608 980813
PRIORITY (CC, No, Date): JP 97230564 970813
DESIGNATED STATES: DE; FR; GB
INTERNATIONAL PATENT CLASS: **G06F-017/60**
ABSTRACT WORD COUNT: 150
NOTE:
Figure number on first page: 1

LANGUAGE (Publication,Procedural,Application): English; English; Japanese
FULLTEXT AVAILABILITY:

| Available Text | Language | Update | Word Count |
|---|---|---|---|
| CLAIMS A | (English) | 9942 | 17239 |
| SPEC A | (English) | 9942 | 160346 |
| Total word count - document A | | | 177585 |
| Total word count - document B | | | 0 |
| Total word count - documents A + B | | | 177585 |

INTERNATIONAL PATENT CLASS: **G06F-017/60**

...SPECIFICATION to the invention cited in claim 17, provided is a mobile electronic commerce system for **paying** , via wireless communication means, a required amount from an electronic wallet that includes the wireless...

**11/3,K/5 (Item 1 from file: 349)**
DIALOG(R)File 349:PCT FULLTEXT
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00986961 **Image available**
**TIMING-INSENSITIVE GLITCH-FREE LOGIC SYSTEM AND METHOD**
**SYSTEME LOGIQUE INSENSIBLE AUX DEFAILLANCES ET AUX PROBLEMES DE SYNCHRONISATION ET PROCEDE ASSOCIE**
Patent Applicant/Assignee:
AXIS SYSTEMS INC, 209 Java Drive, Sunnyvale, CA 94089, US, US (Residence) , US (Nationality), (For all designated states except: US)
Patent Applicant/Inventor:
TSENG Ping-Sheng, 992 Coeur D'Alene Way, Sunnyvale, CA 94087, US, US (Residence), US (Nationality), (Designated only for: US)
LIN Sharon Sheau-Pyng, 10122 Berkshire Court, Cupertino, CA 95014, US, US (Residence), US (Nationality), (Designated only for: US)
SHEN Quincy Kun-Hsu, 19263 Brockton Lane, Saratoga, CA 94070, US, US (Residence), US (Nationality), (Designated only for: US)
Legal Representative:
CHOU Chien-Wei (Chris) (et al) (agent), Oppenheimer Wolff & Donnelly LLP,

1400 Page Mill Road, Palo Alto, CA 94304, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200317148 A1 20030227 (WO 0317148)
Application: WO 2001US25546 20010814 (PCT/WO US0125546)
Priority Application: WO 2001US25546 20010814
Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG US UZ VN YU ZA ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
(OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Publication Language: English
Filing Language: English
Fulltext Word Count: 85087

Main International Patent Class: **G06F-017/50**
Fulltext Availability:
Detailed Description

Detailed Description
... system and software, can be used to produce output files for mapping purposes. The synthesizer **server** 360 has the ability to match the user's **circuit design** components to any standard existing logic elements found in a library 361 (e.g., standard...register components from the FPGA chips into the REG buffer. This process involves a DMA **transfer** of register values in the FPGA chips via the chain of address pointers to the...the DMA engine and the address pointer in the hardware model. The kernel initiates DMA **transfers** together with evaluation requests through direct mapped 1/0 control registers. REG space 317, CLK ...signals to the target system 387. In this in-circuit emulation mode, the hardware model **send** and receive 1/0 signals through the T2H and H2T buffers instead of the S2H...software simulation, the in-circuit emulation mode will also run at a higher speed. The **transmission** of these input and output signals occurs on the PCI bus 328.

Furthermore, a bus...all address pointers associated with a particular address space are chained together. So, during data **transfer** , word data in each chip is sequentially selected ...the software kernel uses the synchronous enable (@
E) and synchronous data (S
D) inputs to
**download** values into the Q port. The S-E port is used as a REG space... software kernel uses the asynchronous enable (A
E) and asynchronous data (A,
D) inputs to
**download** values into the Q port. The A-E port is used as a REG space... to second buffer 517 via wire line 528 to enable the second buffer 517 and **send** the logic "1" value on wire line 529 to the Qoutputonwireline532totheenableinputforregister518. Register518isnowenabledandanydatapresent on wire line...signal is used to initialize the address pointers and begin the word-by-word data **transfer** process.

TheEVAL -...any of the FPGA chips asserts this signal. For example, to evaluate data, data is **transferred** or written from main memory in the host processor's computing station to the FPGAs via the PCI bus. At the end of the **transfer** , the evaluation cycle begins including address pointer initialization and the operation of the software clocks...input

(Local INTI#) 708d, and local data bus 708e.

CTRL FPGA unit 701 contains a **Transfer** Done Checking Logic (XSFR DONE Logic) 1000,
Evaluation Control Logic (EVAL Logic) I 00 1 to all logic elementsiblocks in CTRL
FPGA unit 701.

The **Transfer** Done Checking Logic (XSFR DONE) 1000 receives LAST-SHIFT-H 733, LAST-SHIFT-L 732 and local INTO 708a. XSFR-DONE logic I 000 outputs a **transfer** done signal
(XSFR
DONE) on wireibus 1013 to EVAL Logic 1001. Based on the reception...

...L 732, the XSFR
DONE logic 1 000 checks for the completion of the data **transfer** so that the evaluation cycle can begin, if desired.

The EVAL Logic 1001 receives the XSFR/RD
XSFR
signal on wire/bus 1015, in addition to **transfer** done signal (XSFR-DONE) on wire/bus 1013. EVAL Logic
57
generates two output signals...

...wire/bus 1014 and DATA-XSFR on wirelbus 736. The EVAL logic indicates when data **transfer** between the FPGA bus and the PCI bus will begin to initialize the address pointers. It receives the XSFR-DONE signal when the data **transfer** is complete. The WR-XSFR/RD-XSFR signal indicates whether the **transfer** is a read or a write. Once the 1/0 cycle is complete (or before...descriptor block information corresponding to that in the host memory, including PCI address, local address, **transfer** count, **transfer** direction, and address of the next descriptor block. The host will also set up the address of the initial descriptor block in the descriptor pointer register of the PCI controller. **Transfers** can be initiated by setting a control bit. The PCI loads the first descriptor block and initiates the data **transfer** . The PCI controller continues to load descriptor blocks and **transfer** data until it detects the end of the chain bit is set in the next descriptor pointer register.

Address decoder 1005 receives and **transmits** local R/W control signals on bus 708b, and receives and **transmits** local address signals on bus 708c. The address decoder 1005 generates a write enable signal...The SEM-FPGA R/ W Control logic 1007 controls the various write and read data **transfers** to/from the FPGA low bank and high bank buses.

The DEMLTX logic 1008 is...bottom row to the top row: low bank-high banklow bank-high bank. The data **transfer** chain follows the banks in a predetennined order. The data **transfer** chain for the low bank is shown by arrow 741. The data **transfer** chain for the high bank is shown by arrow 742.

The JTAG configuration chain is...sets up the PCI controller for DMA master read/write modes. Thereafter, the data is **transferred** and verified. Step 807 configures all the FPGA chips with a test design and verifies...not configured or configuration failed
On FPGA configuration is in process
LED3 Red On Data **transfer** is in process.

Off No data **transfer**

At state 1322, the EVALFSMx generates the inputLen signal to the user's design logic to latch the input signals **sent** from the CPU by DMA **transfer** to the user's logic.

**11/3,K/6 (Item 2 from file: 349)**
DIALOG(R)File 349:PCT FULLTEXT
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00982559 **Image available**
**BEHAVIOR PROCESSOR SYSTEM AND METHOD**
**SYSTEME DE PROCESSEUR COMPORTEMENTAL ET PROCEDE ASSOCIE**
Patent Applicant/Assignee:
AXIS SYSTEMS INC, 209 Java Drive, Sunnyvale, CA 94089, US, US (Residence), US (Nationality), (For all designated states except: US)
Patent Applicant/Inventor:
TSENG Ping-sheng, 992 Coeur D'Alene Way, Sunnyvale, CA 94087, US, US (Residence), US (Nationality), (Designated only for: US)
GOEL Yogesh, 44216 Ibero Way, Fremont, CA 94539, US, US (Residence), IN (Nationality), (Designated only for: US)
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LEE James, 745 Boar Circle, Fremont, CA 94539, US, US (Residence), US (Nationality), (Designated only for: US)
SHEN Kun-Hsu, 19263 Brockton Lane, Saratoga, CA 94070, US, US (Residence), US (Nationality), (Designated only for: US)
Legal Representative:
CHOU Chien-Wei (Chris) (agent), Oppenheimer, Wolff & Donnelly LLP, 1400 Page Mill Road, Palo Alto, CA 94304, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200312640 A1 20030213 (WO 0312640)
Application: WO 2001US31794 20011005 (PCT/WO US0131794)
Priority Application: US 2001918600 20010730
Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG US UZ VN YU ZA ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
(OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Publication Language: English
Filing Language: English
Fulltext Word Count: 116802

Main International Patent Class: **G06F-009/455**
Fulltext Availability:
Detailed Description

Detailed Description
... system and software, can be used to produce output files for mapping purposes. The synthesizer **server** 360 has the ability to match the user's **circuit design** components to any standard existing logic elements found in a library 361 (e.g., standard...not configured or configuration failed
On FPGA configuration is in process
LED3 Red On Data **transfer** is in process.

Off No data **transfer**
Blink Diagnostic tests fail

Various other control chips such as the PLX PCI controller 1826...

**11/3,K/7 (Item 3 from file: 349)**
DIALOG(R)File 349:PCT FULLTEXT
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00977214 **Image available**
**APPARATUS AND METHOD FOR CONDITIONING DIGITAL IMAGE DATA FOR DISPLAY OF THE IMAGE REPRESENTED THEREBY**
**APPAREIL ET PROCEDE DE CONDITIONNEMENT DE DONNEES D'IMAGE NUMERIQUES POUR AFFICHER L'IMAGE REPRESENTEE DE CETTE MANIERE**
Patent Applicant/Assignee:
QUALCOMM INCORPORATED, 5775 Morehouse Drive, San Diego, CA 92121, US, US (Residence), US (Nationality)
Inventor(s):
FUDGE Brian, 2425 Aster Street, San Diego, CA 92109, US,
RATZEL John, 12823 Pimpernel Way, San Diego, CA 92129, US,
SCIPIONE Mario, PO Box 7133, Rancho Santa Fe, CA 92067, US,
Legal Representative:
WADSWORTH Philip R (et al) (agent), QUALCOMM Incorporated, 5775 Morehouse Drive, San Diego, CA 92121, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200307226 A1 20030123 (WO 0307226)
Application: WO 2002US21784 20020709 (PCT/WO US0221784)
Priority Application: US 2001901783 20010709
Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO RU SD SE SG SI SK SL TJ TM TN TR TT TZ UA UG UZ VN YU ZA ZM ZW
(EP) AT BE BG CH CY CZ DE DK EE ES FI FR GB GR IE IT LU MC NL PT SE SK TR
(OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZM ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Publication Language: English
Filing Language: English
Fulltext Word Count: 13520

Main International Patent Class: **G06K-009/36**
Fulltext Availability:
Detailed Description

Detailed Description
... sound.

[00051 Digital cinema will encompass many advanced technologies, including digital compression, electronic security methods, **network** architectures and management, **transmission** technologies and cost-effective hardware, **software** and integrated **circuit design** . The technologies necessary for a cost-effective, reliable and secure

**11/3,K/8 (Item 4 from file: 349)**
DIALOG(R)File 349:PCT FULLTEXT
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00975264 **Image available**
**INTER-CHIP COMMUNICATION SYSTEM**
**SYSTEME DE COMMUNICATION INTER-PUCES**
Patent Applicant/Assignee:

AXIS SYSTEMS INC, 209 Java Drive, Sunnyvale, CA 94085, US, US (Residence) , US (Nationality), (For all designated states except: US)
Patent Applicant/Inventor:
TSENG Ping-Sheng, 992 Coeur d'Alene Way, Sunnyvale, CA 94087, US, US (Residence), US (Nationality), (Designated only for: US)
Legal Representative:
CHOU Chien-Wei (Chris) (et al) (agent), Oppenheimer Wolff & Donnelly LLP, 1400 Page Mill Road, Palo Alto, CA 94304, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200305212 A1 20030116 (WO 0305212)
Application: WO 2001US26625 20010823 (PCT/WO US0126625)
Priority Application: US 2001900124 20010706
Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG US UZ VN YU ZA ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
(OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Publication Language: English
Filing Language: English
Fulltext Word Count: 110858

Main International Patent Class: **G06F-013/00**
Fulltext Availability:
Detailed Description

Detailed Description
... component VAX. With the appropriate user interface, the user is capable of simulating the entire **circuit design** using the complete **software** model. Test-bench processes are used to drive the stimulus input, test vector patterns, control...software clock control unit. The array ofFPGAs implements a portion of the user's hardware **circuit design** , as determined above in steps 302-306 of this **software** compilation process. The PCI interface unit allows the reconfigurable hardware emulation model to communicate with...REG, S2H.

H2S, and CLK). In addition to the address pointer and the user's **circuit design** that is modeled and implemented in FPGA chip 450, the MOVE signal generator 470 is...row to the top row: low bank-high bank-low bank-high bank. The data **transfer** chain follows the banks in a predetermined order. The data **transfer** chain for the low bank is shown by arrow 741. The data **transfer** chain for the high bank is shown by arrow 742. The JTAG configuration chain is...sets up the PCI controller for DMA master read/write modes. Thereafter, the data is **transferred** and verified. Step 807 configures all the FPGA chips with a test design and verifies...

**11/3,K/9 (Item 5 from file: 349)**
DIALOG(R)File 349:PCT FULLTEXT
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00967584 **Image available**
**APPARATUS AND METHOD FOR WATERMARKING A DIGITAL IMAGE**
**APPAREIL ET PROCEDE PERMETTANT DE FILIGRANER UNE IMAGE NUMERIQUE**
Patent Applicant/Assignee:
QUALCOMM INCORPORATED, 5775 Morehouse Drive, San Diego, CA 92121-1714, US , US (Residence), US (Nationality)

Inventor(s):
FUDGE Brian, 2425 Aster Street, San Diego, CA 92109, US,
THYAGARAJAN Kadayam, 4782 Thurston Place, San Diego, CA 92130, US,
ROSEN Eric, 611 Calle Paula, Solana Beach, CA 92075, US,
Legal Representative:
OGROD Gregory D (et al) (agent), Qualcomm Incorporated, 5775 Morehouse Drive, San Diego, CA 92121-1714, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 2002101648 A2 20021219 (WO 02101648)
Application: WO 2002US18960 20020613 (PCT/WO US0218960)
Priority Application: US 2001881017 20010613
Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO RU SD SE SG SI SK SL TJ TM TN TR TT TZ UA UG UZ VN YU ZA ZM ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
(OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZM ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Publication Language: English
Filing Language: English
Fulltext Word Count: 15378

Main International Patent Class: **G06T-001/00**
Fulltext Availability:
Detailed Description

Detailed Description
... sound.

[0005] Digital cinema will encompass many advanced technologies, including digital compression, electronic security methods, **network** architectures and management, ' **transmission** technologies and cost-effective hardware, **software** and integrated **circuit design** . The technologies necessary for a cost-effective, reliable and secure system are being analyzed and...

**11/3,K/10 (Item 6 from file: 349)**
DIALOG(R)File 349:PCT FULLTEXT
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00963611 **Image available**
**EXTENDED WEB ENABLED MULTI-FEATURED BUSINESS TO BUSINESS COMPUTER SYSTEM FOR RENTAL VEHICLE SERVICES**
**SYSTEME INFORMATIQUE INTERENTREPRISES A ELEMENTS MULTIPLES A ACCES INTERNET POUR SERVICES DE LOCATION DE VEHICULES**
Patent Applicant/Assignee:
THE CRAWFORD GROUP INC, 600 Corporate Park Drive, St. Louis, MO 63105, US , US (Residence), US (Nationality), (For all designated states except: US)
Patent Applicant/Inventor:
WEINSTOCK Timothy Robert, 1845 Highcrest Drive, St. Charles, MO 63303, US , US (Residence), US (Nationality), (Designated only for: US)
DE VALLANCE Kimberly Ann, 2037 Silent Spring Drive, Maryland Heights, MO 63043, US, US (Residence), US (Nationality), (Designated only for: US)
HASELHORST Randall Allan, 1016 Scenic Oats Court, Imperial, MO 63052, US, US (Residence), US (Nationality), (Designated only for: US)
KENNEDY Craig Stephen, 9129 Meadowglen Lane, St. Louis, MO 63126, US, US (Residence), US (Nationality), (Designated only for: US)

SMITH David Gary, 10 Venice Place Court, Wildwood, MO 63040, US, US (Residence), US (Nationality), (Designated only for: US)
TINGLE William T, 17368 Hilltop Ridge Drive, Eureka, MO 63025, US, US (Residence), US (Nationality), (Designated only for: US)
KLOPFENSTEIN Anita K, 433 Schwarz Road, O'Fallon, IL 62269, US, US (Residence), US (Nationality), (Designated only for: US)
Legal Representative:
HAFERKAMP Richard E (et al) (agent), Howell & Haferkamp, L.C., Suite 1400, 7733 Forsyth Blvd., St. Louis, MO 63105-1817, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200297700 A2 20021205 (WO 0297700)
Application: WO 2001US51431 20011019 (PCT/WO US0151431)
Priority Application: US 2000694050 20001020
Parent Application/Grant:
Related by Continuation to: US 2000694050 20001020 (CIP)
Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PH PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG US UZ VN YU ZA ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
(OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Publication Language: English
Filing Language: English
Fulltext Word Count: 237932

Main International Patent Class: **G06F-017/60**
Fulltext Availability:
Detailed Description

Detailed Description
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**11/3,K/11 (Item 7 from file: 349)**
DIALOG(R)File 349:PCT FULLTEXT
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00933152 **Image available**
**EXTENDED WEB ENABLED MULTI-FEATURED BUSINESS TO BUSINESS COMPUTER SYSTEM FOR RENTAL VEHICLE SERVICES**
**SYSTEME INFORMATIQUE ETENDU ENTRE ENTREPRISES, A FONCTIONS MULTIPLES, FONCTIONNANT SUR LE WEB, POUR DES SERVICES DE LOCATION DE VEHICULES**
Patent Applicant/Assignee:
THE CRAWFORD GROUP INC, 600 Corporate Park Drive, St. Louis, MO 63105, US , US (Residence), US (Nationality), (For all designated states except: US)
Patent Applicant/Inventor:
WEINSTOCK Timothy Robert, 1845 Highcrest Drive, St. Charles, MO 63303, US , US (Residence), US (Nationality), (Designated only for: US)
DE VALLANCE Kimberly Amm, 2037 Silent Spring Drive, Maryland Heights, MO 63043, US, US (Residence), US (Nationality), (Designated only for: US)
HASELHORST Randall Allan, 1016 Scenic Oats Court, Imperial, MO 63052, US, US (Residence), US (Nationality), (Designated only for: US)
KENNEDY Craig Stephen, 9129 Meadowglen Lane, St. Louis, MO 63126, US, US

(Residence), US (Nationality), (Designated only for: US)
SMITH David Gary, 10 Venice Place Court, Wildwood, MO 63040, US, US (Residence), US (Nationality), (Designated only for: US)
TINGLE William T, 17368 Hilltop Ridge Drive, Eureka, MO 63025, US, US (Residence), US (Nationality), (Designated only for: US)
KLOPFENSTEIN Anita K, 433 Schwarz Road, O'Fallon, IL 62269, US, US (Residence), US (Nationality), (Designated only for: US)
Legal Representative:
HAFERKAMP Richard E (et al) (agent), HOWELL & HAFERKAMP, L.C., Suite 1400, 7733 Forsyth Blvd., St. Louis, MO 63105-1817, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200267175 A2 20020829 (WO 0267175)
Application: WO 2001US51437 20011019 (PCT/WO US0151437)
Priority Application: US 2000694050 20001020
Parent Application/Grant:
Related by Continuation to: US 2000694050 20001020 (CIP)
Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PH PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG US UZ VN YU ZA ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
(OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Publication Language: English
Filing Language: English
Fulltext Word Count: 243912

Main International Patent Class: **G06F-017/60**

**11/3,K/12 (Item 8 from file: 349)**
DIALOG(R)File 349:PCT FULLTEXT
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00886047
**SYSTEM, METHOD, USES, PRODUCTS, PROGRAM PRODUCTS, AND BUSINESS METHODS FOR DISTRIBUTED INTERNET AND DISTRIBUTED NETWORK SERVICES**
**SYSTEME, PROCEDE, UTILISATIONS, PRODUITS, PRODUITS PROGRAMMES ET PROCEDES COMMERCIAUX POUR INTERNET REPARTI ET SERVICES DE RESEAU REPARTIS**
Patent Applicant/Assignee:
INTERNATIONAL INTERACTIVE COMMERCE LTD, 84 Business Park, Suite 305, Armonk, NY 10504, US, US (Residence), US (Nationality), (For all designated states except: US)
Patent Applicant/Inventor:
CHEN Shuang, 208 Briarwood Drive, Somers, NY 10589, US, US (Residence), US (Nationality), (Designated only for: US)
PIZZORNI Paolo R, 1502 Frontier Drive, Arlington, TX 76012, US, US (Residence), US (Nationality), (Designated only for: US)
RUBIN William B, 18 Eagle Lane, Poughkeepsie, NY 12601-1203, US, US (Residence), US (Nationality), (Designated only for: US)
PACE Charles P, 70 Smith Farm Road, North Chittenden, VT 05763, US, US (Residence), US (Nationality), (Designated only for: US)
DE FOREST Darin S, 1418 E. Briarwood Terrace, Phoenix, AZ 85048, US, US (Residence), US (Nationality), (Designated only for: US)
BOBICK Mark, 138 Myrtle Avenue, P.O. Box 87, Mahopac Falls, NY 10542, US, US (Residence), US (Nationality), (Designated only for: US)
Legal Representative:
BIRDE Patrick J (et al) (agent), Kenyon & Kenyon, One Broadway, New York, NY 10004, US,
Patent and Priority Information (Country, Number, Date):

Patent: WO 200219063 A2 20020307 (WO 0219063)
Application: WO 2001US27522 20010904 (PCT/WO US0127522)
Priority Application: US 2000229685 20000901; US 2000236864 20000929; US 2000237179 20001002; US 2000254377 20001208; US 2001262288 20010117
Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PH PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG US UZ VN YU ZA ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
(OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Publication Language: English
Filing Language: English
Fulltext Word Count: 139605

Main International Patent Class: **G06F**
Fulltext Availability:
Detailed Description

Detailed Description
SYSTEM, METHOD, USES, PRODUCTS,
**PROGRAM** PRODUCTS., AND BUSINESS METHODS FOR
DISTRIBUTED **INTERNET** AND DISTRIBUTED **NETWORK** SERVICES
PRIORITY DOCUMENTS & RELATED REFERENCES
This application claims priority to provisional U.S. Patent Application
...

**11/3,K/13 (Item 9 from file: 349)**
DIALOG(R)File 349:PCT FULLTEXT
(c) 2003 WIPO/Univentio. All rts. reserv.

00870041 **Image available**
**NETWORK-BASED PHOTOMASK DATA ENTRY INTERFACE AND INSTRUCTION GENERATOR FOR MANUFACTURING PHOTOMASKS**
**INTERFACE D'ENTREES DE DONNEES DE MASQUES DE PHOTOGRAVURE BASEE SUR RESEAU ET GENERATEUR D'INSTRUCTIONS DESTINEES A LA FABRICATION DE MASQUES DE PHOTOGRAVURE**
Patent Applicant/Assignee:
DUPONT PHOTOMASKS INC, 131 Old Settlers Boulevard, Round Rock, TX 78664, US, US (Residence), US (Nationality)
Inventor(s):
COGDELL Thomas T, 2200 Canterbury Street, Austin, TX 78702, US,
SCHEPP Jeffry S, 1708 Crestline Court, Round ROck, TX 78664, US,
GENTRY Jan E, 310 Highland Estates, Round Rock, TX 78664, US,
Legal Representative:
FELGER Thomas R (agent), Baker Botts L.L.P., 2001 Ross Avenue, Suite 600, Dallas, TX 75201-2980, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200203141 A2-A3 20020110 (WO 0203141)
Application: WO 2001US21020 20010629 (PCT/WO US0121020)
Priority Application: US 2000610917 20000705
Designated States: AE AG AL AM AT (utility model) AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ (utility model) DE (utility model) DK (utility model) DM DZ EC EE (utility model) ES FI (utility model) GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK (utility model) SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR

(OA) BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Publication Language: English
Filing Language: English
Fulltext Word Count: 4715

Main International Patent Class: **G06F-017/30**
Fulltext Availability:
Detailed Description

Detailed Description
... could establish a connection to a web site.

Various user interface screens described herein are **downloaded** to customer computer 102. Interface computer 108 would receive the photomask data that the customer...

...network; only the end stations are illustrated in FIGURE 1A. In the case of an **Internet** connection, customer computer 102 need not have special **programming** other than a **web** browser.

The customer also has a **circuit design** computer 104.

**Circuit design** computer 104 stores **programming** for generating designs the customer's integrated circuit. It is possible that computers 102 and...

**11/3,K/14 (Item 10 from file: 349)**
DIALOG(R)File 349:PCT FULLTEXT
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00855097 **Image available**
**ELECTRONIC PRODUCT DESIGN SYSTEM**
**SYSTEME ELECTRONIQUE DE CONCEPTION DE PRODUITS**
Patent Applicant/Inventor:
BROWN Don, 1745 Appaloosa Road, Warrington, VA 18976, US, US (Residence), US (Nationality)
Legal Representative:
GREENBAUM Michael C (et al) (agent), Blank Rome Comisky & McCauley LLP, 900 17th Street, N.W., Suite 1000, Washington, DC 20006, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200188759 A1 20011122 (WO 0188759)
Application: WO 2001US15282 20010511 (PCT/WO US0115282)
Priority Application: US 2000570027 20000512
Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CR CU CZ DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
(OA) BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Publication Language: English
Filing Language: English
Fulltext Word Count: 12969

Main International Patent Class: **G06F-017/30**

Fulltext Availability:
Detailed Description

Detailed Description
... after data results are made available to the user, the vendor-supplied data can be **downloaded** from the vendor database into the user's workstation. Since the vendorsupplied data is provided...

...supplied data can then be imported from the vendor-supplied database direaly into any desired **EDA** design tool. The import can be achieved with either import **software** supplied at the EPDeS **web** site or else*here or by virtue of the import features made available by the...

**11/3,K/15 (Item 11 from file: 349)**
DIALOG(R)File 349:PCT FULLTEXT
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00831835 **Image available**
**AUTOMATED METHOD AND SYSTEM FOR SELECTING AND PROCURING ELECTRONIC COMPONENTS USED IN CIRCUIT AND CHIP DESIGNS**
**PROCEDE ET SYSTEME AUTOMATISES POUR SELECTIONNER ET OBTENIR DES COMPOSANTS ELECTRONIQUES UTILISES DANS LA CONCEPTION DE CIRCUITS INTEGRES ET DE PUCES**
Patent Applicant/Assignee:
CADENCE DESIGN SYSTEMS INC, 2655 Seely Avenue, San Jose, CA 95134, US, US (Residence), US (Nationality)
Inventor(s):
ROBERTSON William H, 1574 Kathy Lane, Los Altos, CA 94024, US,
PLYMALE James M, 10145 SW Redwing Terrace, Beaverton, OR 97007, US,
Legal Representative:
VANDERLAAN Christopher A (et al) (agent), Lyon & Lyon LLP, Suite 4700, 633 West Fifth Street, Los Angeles, CA 90071, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200165423 A2-A3 20010907 (WO 0165423)
Application: WO 2001US6155 20010226 (PCT/WO US0106155)
Priority Application: US 2000514674 20000228
Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CR CU CZ DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
(OA) BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Publication Language: English
Filing Language: English
Fulltext Word Count: 8239

Main International Patent Class: **G06F-017/50**
Fulltext Availability:
Claims

Claim
... electronic design.

16 The system of claim 15, wherein said dynamic parts fimction within said **application** as components of a modeled **electronic design** .

17 The system of claim 14, wherein said **server transmits** a list of

dynamic parts to the user computer for graphical display, and receives a ...

**11/3,K/16 (Item 12 from file: 349)**
DIALOG(R)File 349:PCT FULLTEXT
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00831834 **Image available**
**METHOD AND SYSTEM FOR FACILITATING ELECTRONIC CIRCUIT AND CHIP DESIGN USING REMOTELY LOCATED RESOURCES**
**PROCEDE ET SYSTEME D'ASSISTANCE A LA CONCEPTION DE CIRCUITS ELECTRONIQUES ET DE PUCES FAISANT APPEL A DE RESSOURCES ELOIGNEES**
Patent Applicant/Assignee:
CADENCE DESIGN SYSTEMS INC, 2655 Seely Avenue, San Jose, CA 95134, US, US (Residence), US (Nationality)
Inventor(s):
ROBERTSON William H, 1574 Kathy Lane, Los Altos, CA 94024, US,
PLYMALE James M, 10145 SW Redwing Terrace, Beaverton, OR 97007, US,
Legal Representative:
VANDERLAAN Christopher A (et al) (agent), Lyon & Lyon LLP, Suite 4700, 633 West Fifth Street, Los Angeles, CA 90071-2066, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200165422 A2-A3 20010907 (WO 0165422)
Application: WO 2001US6141 20010226 (PCT/WO US0106141)
Priority Application: US 2000514757 20000228
Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CR CU CZ DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
(OA) BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Publication Language: English
Filing Language: English
Fulltext Word Count: 20218

Main International Patent Class: **G06F-017/50**
Fulltext Availability:
Detailed Description

Detailed Description
... adapted to allow the user to put together a series of scripts so as to **program** the usage of one or more **EDA** tools, which may be accessed, as needed, via the **portal** site 204. For example, a user might program a script for a design compiling process...

**11/3,K/17 (Item 13 from file: 349)**
DIALOG(R)File 349:PCT FULLTEXT
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00806384
**NETWORK AND LIFE CYCLE ASSET MANAGEMENT IN AN E-COMMERCE ENVIRONMENT AND METHOD THEREOF**
**GESTION D'ACTIFS DURANT LE CYCLE DE VIE ET EN RESEAU DANS UN ENVIRONNEMENT DE COMMERCE ELECTRONIQUE ET PROCEDE ASSOCIE**
Patent Applicant/Assignee:
ACCENTURE LLP, 1661 Page Mill Road, Palo Alto, CA 94304, US, US

(Residence), US (Nationality)
Inventor(s):
MIKURAK Michael G, 108 Englewood Blvd., Hamilton, NJ 08610, US,
Legal Representative:
HICKMAN Paul L (agent), Oppenheimer Wolff & Donnelly, LLP, 38th Floor, 2029 Century Park East, Los Angeles, CA 90067-3024, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200139030 A2 20010531 (WO 0139030)
Application: WO 2000US32324 20001122 (PCT/WO US0032324)
Priority Application: US 99444775 19991122; US 99447621 19991122
Designated States: AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CU CZ DE DK DZ EE ES FI GB GE GH GM HR HU ID IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG UZ VN YU ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
(OA) BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Publication Language: English
Filing Language: English
Fulltext Word Count: 171499

Main International Patent Class: **G06F-017/60**
Fulltext Availability:
Detailed Description

Detailed Description
... represent physical objects, such as automobiles in a traffic-flow simulation, electrical components in a **circuit - design program** , countries in an economics model, or aircraft in an air-traffic-control system.

Objects can...such as, the creation of an order or trouble ticket or the adjustment of a **bill** . This process logs customer contacts, directs inquiries to the appropriate party, and tracks the status...requests, and/or usage requests.
Finally, in step 2006, a network process to which to **send** the generated data is identified.

Figure 21 shows a block diagram of the Problem Handling...processing their payments and performing payment collections. In addition, this process handles customer inquiries about **bills** , and is responsible to resolve billing problems to the customer's satisfaction. The aim is to provide a correct **bill** and, if there is a billing problem, resolve it quickly with appropriate status to the...

...initiates a use of the hybrid network, the hybrid network, in a first step 2700, **transfers** the media over the network using IP information to route it to the appropriate destination. The media **transferred** over the network may be telephony data, image data, or any other data capable of packet switched **transmission** .

In a second step 2702, events are generated based on the quality of service of the media **transfer** . As discussed above with reference to Figure 17 and Figure 19, these events include performance...

...a third step 2704, the events generated in step 2702 are utilized to generate a **bill** for the customer. In addition to normal billing for service provided via the hybrid network, the **bill** is modified based on events generated during the media **transfer** . For example, events

...3.0, March 1996, and hereby
incorporated by reference. SSL provides a means for secure **transmission** between two computers. SSL has the advantage that it does not require specialpurpose software to...

...gateway but not to the merchant. Although SSL allows for- robustly secure two-party data **transmission** , it does not meet the ultimate need of the electronic commerce market for robustly secure three-party data **transmission** .

Other examples of general-purpose secure communication protocols include Private Communications Technology ("PCT") from Microsoft...

...that any of the general-purpose secure communication protocols can be substituted for the SSL **transmission** protocol without undue experimentation.

Banks desire an Internet payment solution that emulates existing Point of ...servers
distribute the HTML formatted documents using a specific communication protocol known as the HyperText **Transfer** Protocol (HTTP).

To access the multi-media information available on World-Wide Web servers, a...

...all or parts of a useful publicly accessible online system. Second, the online service may **pay** the user for performing some type of action such as winning a contest or completing...be provided on a for-fee basis. Conversely, an online service provider may wish to **pay** third party content providers for placing useful material on the online service.

Thus, when creating...

...containing greater detail or to a purchasing area.

169
The use of advertising revenues to **pay** for information dissemination is well established in domains such as television and radio in which...the order is placed with a provider of an ordered service.

Optionally, notification may be **sent** to the user to notify the user that the
transaction is being completed or confirmation that the order has been completed. Also optionally, a tracking number may be **sent** to the user for assisting a user to determine the shipping status of a product...

**11/3,K/18 (Item 14 from file: 349)**
DIALOG(R)File 349:PCT FULLTEXT
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00761432
**METHODS, CONCEPTS AND TECHNOLOGY FOR DYNAMIC COMPARISON OF PRODUCT FEATURES AND CUSTOMER PROFILE**
**PROCEDES, CONCEPTS ET TECHNIQUE DE COMPARAISON DYNAMIQUE DE CARACTERISTIQUES D'UN PRODUIT ET DU PROFIL DES CONSOMMATEURS**
Patent Applicant/Assignee:
ANDERSEN CONSULTING LLP, 100 South Wacker Drive, Chicago, IL 60606, US,
US (Residence), US (Nationality)

Inventor(s):
GUHEEN Michael F, 2218 Mar East Street, Tiburon, CA 94920, US
MITCHELL James D, 3004 Alma, Manhattan Beach, CA 90266, US
BARRESE James J, 757 Pine Avenue, San Jose, CA 95125, US
Legal Representative:
BRUESS Steven C, Merchant & Gould P.C., P.O. Box 2903, Minneapolis, MN 55402-0903, US
Patent and Priority Information (Country, Number, Date):
Patent: WO 200073958 A2 20001207 (WO 0073958)
Application: WO 2000US14459 20000524 (PCT/WO US0014459)
Priority Application: US 99320818 19990527
Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY CA CH CN CR CU CZ DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
(OA) BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Publication Language: English
Filing Language: English
Fulltext Word Count: 151011

Main International Patent Class: **G06F-017/60**
Fulltext Availability:
Detailed Description

Detailed Description
... capture both the small scale patterns and major mechanisms that implement the common requirements and **design** in a specific **application** domain. They were first developed to free **application programmers** from the chores involved in displaying menus, windows, dialog boxes, and other standard user interface...applications receive data from the event/data generation, event processing, and repositories components and then **send** data to the presentation or repositories components. Management applications tools include capacity planning tools, performance...accounting information for calculating actual costs, determines chargeback costs based on pre-defined algorithms and **bills** users for service rendered.

194
Billing & Accounting also makes payments to service providers for services...

...in accordance with agreed upon SLAs. As part of this payment process Billing & Accounting reconciles **bills** from service providers against monitored costs and SLA/OLA violations.

Systems Management Planning (1330)
Capacity...

**11/3,K/19 (Item 15 from file: 349)**
DIALOG(R)File 349:PCT FULLTEXT
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00761429
**METHODS, CONCEPTS AND TECHNOLOGY FOR A VIRTUAL SHOPPING SYSTEM CAPABLE OF ASSESSING NEEDS OF A CUSTOMER AND RECOMMENDING A PRODUCT OR SERVICE BASED ON SUCH ASSESSED NEEDS**

**PROCEDES, CONCEPTS ET TECHNOLOGIE POUR SYSTEME D'ACHAT VIRTUEL CAPABLE D'EVALUER LES BESOINS D'UN CLIENT ET DE RECOMMANDER UN PRODUIT OU UN SERVICE SUR LA BASE DE CES BESOINS**

Patent Applicant/Assignee:
ACCENTURE LLP, 100 South Wacker Drive, Chicago, IL 60606, US, US (Residence), US (Nationality)
Inventor(s):
GUHEEN Michael F, 2218 Mar East Street, Tiburon, CA 94920, US,
MITCHELL James D, 3004 Alma, Manhattan Beach, CA 90266, US,
BARRESE James J, 757 Pine Avenue, San Jose, CA 95125, US,
Legal Representative:
BRUESS Steven C (agent), Merchant & Gould P.C., P.O. Box 2903, Minneapolis, MN 55402-0903, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200073955 A2 20001207 (WO 0073955)
Application: WO 2000US14357 20000524 (PCT/WO US0014357)
Priority Application: US 99321495 19990527
Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY CA CH CN CR CU CZ DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
(OA) BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Publication Language: English
Filing Language: English
Fulltext Word Count: 148469

Main International Patent Class: **G06F-017/60**
Fulltext Availability:
Detailed Description

Detailed Description
... represent physical objects, such as automobiles in a traffic-flow simulation, electrical components in a **circuit - design program** , countries in an economics model, or aircraft in an air-traffic-control system.
0 Objects...applications receive data from the event/data generation, event processing, and repositories components and then **send** data to the presentation or repositories components. Management applications tools include capacity planning tools, performance...accounting information for calculating actual costs, determines chargeback costs based on pre-defined algorithms and **bills** users for service rendered.

Billing & Accounting also makes payments to service providers for services and...

...in accordance with agreed upon SLAs. As part of this payment process Billing & Accounting reconciles **bills** from service providers against monitored costs and SLA/OLA violations.

Systems Management Planning (1330)
CaVacily...and remote printing, and distribution management through a software package or an equivalent alternative.

File **Transfer** & Control
File **Transfer** and Control initiates and monitors files being **transferred** throughout the system as part of the business processing (e.g., nightly batch runs). File **transfers** may occur between any two or

more devises within the system.

System Startup & Shutdown
System...

**11/3,K/20 (Item 16 from file: 349)**
DIALOG(R)File 349:PCT FULLTEXT
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00761422
**BUSINESS ALLIANCE IDENTIFICATION**
**SYSTEME, PROCEDE ET ARTICLE DE PRODUCTION POUR L'IDENTIFICATION D'ALLIANCES COMMERCIALES DANS UN CADRE D'ARCHITECTURE RESEAU**
Patent Applicant/Assignee:
ACCENTURE LLP, 100 South Wacker Drive, Chicago, IL 60606, US, US (Residence), US (Nationality)
Inventor(s):
GUHEEN Michael F, 2218 Mar East Street, Tiburon, CA 94920, US,
MITCHELL James D, 3004 Alma, Manhattan Beach, CA 90266, US,
BARRESE James J, 757 Pine Avenue, San Jose, CA 95125, US,
Legal Representative:
BRUESS Steven C (agent), Merchant, Gould, Smith, Edell, Welter & Schmidt, P.A., P.O. Box 2903, Minneapolis, MN 55402-0903, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200073928 A2-A3 20001207 (WO 0073928)
Application: WO 2000US14375 20000524 (PCT/WO US0014375)
Priority Application: US 99320816 19990527
Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY CA CH CN CR CU CZ DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
(OA) BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Publication Language: English
Filing Language: English
Fulltext Word Count: 149371

Main International Patent Class: **G06F-017/60**
Fulltext Availability:
Detailed Description

Detailed Description
... represent physical objects, such as automobiles in a traffic-flow simulation, electrical components in a **circuit - design program** , countries in an economics model, or aircraft in an air-traffic-control system.

0 Objects...applications receive data from the event/data generation, event processing, and repositories components and then **send** data to the presentation or repositories components. Management applications tools include capacity planning tools, perforinance...accounting inforination for calculating actual costs, determines chargeback costs based on pre-defined algorithms and **bills** users for service rendered.

Billing & Accounting also makes payments to service providers for services and...

...in accordance with agreed upon SLAs. As part of this payment process Billing & Accounting reconciles **bills** from service providers against monitored costs and SLA/OLA violations.

Systems Management Planning (1330)
Capacity...and remote printing, and distribution management through a software package or an equivalent alternative.

File **Transfer** & Control
File **Transfer** and Control initiates and monitors files being **transferred** throughout the system as part of the business processing (e.g., nightly batch runs). File **transfers** may occur between any two or more devises within the system.

System Startgp & Shutdown
System...

**11/3,K/21 (Item 17 from file: 349)**
DIALOG(R)File 349:PCT FULLTEXT
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00759623
**BEHAVIORAL-SYNTHESIS ELECTRONIC DESIGN AUTOMATION TOOL AND BUSINESS-TO-BUSINESS APPLICATION SERVICE PROVIDER**
**FOURNISSEUR DE SERVICE DE LOGICIEL PASSE-PARTOUT COMPORTANT UN OUTIL D'AUTOMATISATION DE LA CONCEPTION ELECTRONIQUE A SYNTHESE COMPORTEMENTALE**
Patent Applicant/Assignee:
GET2CHIP, 2107 N. First Street, Suite 350, San Jose, CA 95131, US, US (Residence), US (Nationality)
Inventor(s):
FRANK Elof, 378 America Avenue, Sunnyvale, CA 94086, US,
BRAUNE Bernd, 624 Fremont Avenue, Menlo Park, CA 94025, US,
KNAPP David, 1281 Goose Point Common, San Jose, CA 95131, US,
FERNANDES Pradeep, 3918 Mylinda Drive, San Jose, CA 95132, US,
SCHMIDT Hans-Joachim, Wahnfriedallee 1B, D-81925 Munchen, DE,
Legal Representative:
GLENN Michael A (et al) (agent), Glenn Patent Group, 3475 Edison Way, Suite L, Menlo Park, CA 94025, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200072185 A2-A3 20001130 (WO 0072185)
Application: WO 2000US14617 20000526 (PCT/WO US0014617)
Priority Application: US 99136127 19990526; US 99135902 19990526; US 99136126 19990526; US 2000574572 20000517; US 2000574693 20000517; US 2000577426 20000522; US 2000579825 20000525
Designated States: AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG UZ VN YU ZA ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
(OA) BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Publication Language: English
Filing Language: English
Fulltext Word Count: 12464

Main International Patent Class: **G06F-017/50**
Fulltext Availability:

Detailed Description
Claims

English Abstract
A business-to-business **application** service provider includes an **Internet website** and **webserver** with **EDA** -on-demand solutions for system-on-a-chip designers. Such **website** allows wlectronic designs in hardware description language to be **uploaded** into a front-end EDA design environment. A behavioral model simulation tool hosted privately on...

...secure environment of the business-to-business application service provider. The validated solubtion is then **downloaded** back over the Internet for a **pay** -per- **use** fee to the customer, and in a form ready to be placed and routed by a back-end **EDA** tool. Such validated design solutions are also **downloadable** to others in exchange for other designs, or available in technology libraries. The intellectual property ...

Detailed Description
... application service provider. The validated solution is then downloaded back over the Internet for a **pay** -per- **use** fee to the customer, in a form ready to be placed and routed by a back-end **EDA** tool. Such validated design solutions are also **downloadable** to others in exchange for other designs, or available i-1 technology libraries. The intellectual...with, e.g., WINDOWS-NT, IIS, and ASP, commercial software from Microsoft to host client web browser visits. A **pay** -per- **use electronic design** automation ( **EDA** ) tool 108 is installed as a **software application** on the **webserver** 106. Any of a number of users and customers are represented by a web client...

...browser 1 1 2. An architect's electronic design in hardware description language (HIDL) is **uploaded** over the Internet 102 for simulation and design verification by the EDA tool 108. Once complete, the verified result is
SUBSTITUTE SHEET (RULE 26)
**downloaded** back to a place back-end process 114 and a route back-end process 116...

Claim
... front-end electronic design automation (EDA) tool, and connected to receive said HIDL;
and
a **subscription** controller that provides for a billing of said system-on-a-chip designer as a condition of **downloading** back a simulated and verified derivative of said
**electronic design** over the Internet;
1 5 wherein, users of said EDA-on-demand solution are charged a **pay** -per- **use** fee to create a unique intellectual property.

2 The business-to-business application service provider...

**11/3,K/22 (Item 18 from file: 349)**
DIALOG(R)File 349:PCT FULLTEXT
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00579162 **Image available**
**MULTITHREADED HDL LOGIC SIMULATOR**
**SIMULATEUR LOGIQUE MULTIFILIERE DU HDL**

Bode Akintola 20-May-03

Patent Applicant/Assignee:
  CHAN Terence,
Inventor(s):
  CHAN Terence,
Patent and Priority Information (Country, Number, Date):
  Patent:  WO 200042535 A1 20000720 (WO 0042535)
  Application:  WO 2000US853 20000112  (PCT/WO US0000853)
  Priority Application: US 99229134 19990112
Designated States: AE AL AM AT AU AZ BA BB BG BR BY CA CH CN CR CU CZ DE DK
  DM EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR
  LS LT LU LV MA MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ
  TM TR TT TZ UA UG US UZ VN YU ZA ZW GH GM KE LS MW SD SL SZ TZ UG ZW AM
  AZ BY KG KZ MD RU TJ TM AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL
  PT SE BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
Publication Language: English
Fulltext Word Count: 23800

Main International Patent Class:  **G06F-017/50**
Fulltext Availability:
  Claims

Claim
... according to claim
  fur-Lhcr compriseto the step of providing an interFace function to
  support **network** transports and 1COMMUlliCation bet-ween the UT arid
  the servor **program** .
  3 B. The met-hod of executing remotc **Hardware** **Descriptim** Lariguage
  ('111ML,I) Compilation and logic sjiiiulation accorcli.nq to claim 37
  wherein the step...

...interface
  furict..J.uxl to support network transports and communication etweerx
  the UI and the **server** proqram,
  42
  . The **program** prOdUCt C):[-' H--Xe-C-Uting remote **Hardware**
  **Description**
  Lanquage ("IlDL") compilation and logic r.@imulation according to
  claim 40 wherein the user, s...3 UOTqPTnUITS @[Ggs=14 ATTPDTqpwoqne oq
  sup9w (P)
  CS800100sfillad SESU/00 Om
  (f) installing a **server** **program** on the remote hosts to
  which the **HDL** logic simulation is to be performed by the
  simulator **networked** through Internet or intranets.

  85 The method of providing job scheduling for Hardware
  Description Language...

**11/3,K/23  (Item 19 from file: 349)**
DIALOG(R)File 349:PCT FULLTEXT
(c) 2003 WIPO/Univentio. All rts. reserv.

00554539  **Image available**
**A PROTOTYPING SYSTEM AND A METHOD FOR OPERATING THE SAME**
**SYSTEME DE PROTOTYPAGE ET SON PROCEDE DE FONCTIONNEMENT**
Patent Applicant/Assignee:
  YANG Sei-Yang,
Patent and Priority Information (Country, Number, Date):
  Patent:  WO 200017912 A2 20000330 (WO 0017912)
  Application:  WO 99KR571 19990920  (PCT/WO KR9900571)

Priority Application: KR 9838834 19980919
Designated States: AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
Publication Language: English
Fulltext Word Count: 16230

Main International Patent Class: **G06F-017/50**
International Patent Class: **G06F-017/00** ...

... **G06F-019/00**
Fulltext Availability:
Detailed Description

Detailed Description
... circuit (called additional circuit for R-communication, and wiH be explained later)
which is to **transmit** signal values among the RFPDs. The **server** computer
partitions the **designed** **circuit** to be verified with partial circuits by executing prototyping system **software** , allocates the partitioned partial circuits to the respective RFPDs or other component devices 'in the...

**11/3,K/24** **(Item 20 from file: 349)**
DIALOG(R)File 349:PCT FULLTEXT
(c) 2003 WIPO/Univentio. All rts. reserv.

00254744
**NETWORK ADAPTER WITH HOST INDICATION OPTIMIZATION**
**ADAPTATEUR DE RESEAU AVEC OPTIMISATION DES INDICATIONS DU SYSTEME CENTRAL**
Patent Applicant/Assignee:
3COM CORPORATION,
Inventor(s):
PETERSEN Brian,
SHERER W Paul,
BROWN David R,
LO Lai-Chin,
Patent and Priority Information (Country, Number, Date):
Patent: WO 9402900 A1 19940203
Application: WO 93US7056 19930727 (PCT/WO US9307056)
Priority Application: US 92898 19920728
Designated States: AU CA JP AT BE CH DE DK ES FR GB GR IE IT LU MC NL PT SE
Publication Language: English
Fulltext Word Count: 26080

Main International Patent Class: **G06F-013/00**
Fulltext Availability:
Detailed Description

Detailed Description
... processor 5 responds to network adapter 3 before a
1 0 complete data frame is **transferred** , host processor 5 then may decrease the threshold value in alterable storage location 1 Oa...

...logic 1 0 to generate the indication signal at a later time in the next **transfer** of a data frame. Alternatively, if host processor 5 responds to the network adapter 3 after a complete data frame has
1 5 already been **transferred** , host processor 5 may then increase the threshold value in alterable storage location 1 Oa...

...the
threshold logic to generate an indication signal at an earlier time in the
next **transfer** of a data frame,
I . System Overview
Fig. 3 is a schematic diagram of host...

...with the
network interface adapter of the present invention. The network interface controller includes a **network** interface processor 14, implemented in one preferred system as an **application** specific integrated **circuit** **designed** to implement the functions outlined below using VERILOG design tools as known in the art...

**11/3,K/25 (Item 21 from file: 349)**
DIALOG(R)File 349:PCT FULLTEXT
(c) 2003 WIPO/Univentio. All rts. reserv.

00254735
**APPARATUS FOR AUTOMATIC INITIATION OF DATA TRANSMISSION**
**APPAREIL DE DECLENCHEMENT AUTOMATIQUE DE TRANSMISSIONS DE DONNEES**
Patent Applicant/Assignee:
3COM CORPORATION,
Inventor(s):
PETERSEN Brian,
BROWN David R,
Patent and Priority Information (Country, Number, Date):
Patent: WO 9402891 A1 19940203
Application: WO 93US7060 19930727 (PCT/WO US9307060)
Priority Application: US 92893 19920728
Designated States: AU CA JP AT BE CH DE DK ES FR GB GR IE IT LU MC NL PT SE
Publication Language: English
Fulltext Word Count: 17765

Main International Patent Class: **G06F-003/00**
International Patent Class: **G06F-11:00**
Fulltext Availability:
Claims
Claim
... frame has been transferred from the host computer 30 into the buffer

34 if the **transmit** logic 39 is available to **transmit** the frame subject
of the ongoing **download** from the host computer 30, the frame being **downloaded** into the buffer 34 is larger than the threshold set by the threshold store 43, and the host computer 30 indicates that immediate **transmission** of the data is desired.
As mentioned above, the buffer 34 may be directly addressable...

...space into which the host computer 30 writes data
and control signals associated with a **transmission** operation. The host interface 31 then maps the **transfer** of data from that prespecified address space into the buffer 34 and host accessible registers...

...a host system address space of about 4
Gigabytes.
The network interface controller includes a **network** interface processor 14, implemented in one preferred system as an **application**

specific integrated **circuit designed** to implement the functions outlined below using VERILOG design tools as known in the art...

```
Set     Items   Description
S1    1301752   APPLICATION? OR SOFTWARE? OR PROGRAM? OR FREEWARE? OR SHAR-
            EWARE?
S2      15888   EDA OR (ELECTRONIC? OR CIRCUIT?)(1N)DESIGN? OR HDL OR HARD-
            WARE()DESCRIPT?
S3      97148   SUBSCRIB? OR SUBSCRIPTION OR PAY??? OR BILL? ? OR PAY(2N)(-
            USE OR USAGE)
S4    2812646   UPLOAD? OR DOWNLOAD? OR TRANSFER? OR TRANSMI? OR SENT OR S-
            END?
S5     518028   ONLINE OR ON()LINE OR INTERNET OR INTRANET OR WEB? OR HOME-
            PAGE OR HOME()PAGE OR NETWORK? OR PORTAL? OR WWW OR CYBER? OR
            LAN OR WAN OR SERVER?
S6          3   S1 AND S2 AND S3 AND S4 AND S5
S7        818   S1(10N)S2
S8         28   S7(15N)S5
S9        738   S2(15N)S4
S10         7   S9(15N)S3
S11        28   (S6 OR S8 OR S10) AND IC=G06F?
? show file
File 344:Chinese Patents Abs Aug 1985-2003/Feb
         (c) 2003 European Patent Office
File 347:JAPIO Oct 1976-2003/Jan(Updated 030506)
         (c) 2003 JPO & JAPIO
File 350:Derwent WPIX 1963-2003/UD,UM &UP=200331
         (c) 2003  Thomson Derwent
File 371:French Patents 1961-2002/BOPI 200209
         (c) 2002 INPI.  All rts. reserv.
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Bode Akintola  20-May-03

**11/5/1 (Item 1 from file: 347)**
DIALOG(R)File 347:JAPIO
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07189276 **Image available**
COMMUNICATION **NETWORK** **DESIGN** **CIRCUIT** , **DESIGN** METHOD THEREFOR, RECORDING MEDIUM HAVING CONTROL **PROGRAM** RECORDED THEREON AND TRANSMISSION MEDIUM

PUB. NO.: 2002-057676 [JP 2002057676 A]
PUBLISHED: February 22, 2002 (20020222)
INVENTOR(s): SAITO HIROYUKI
APPLICANT(s): NEC CORP
APPL. NO.: 2000-240546 [JP 2000240546]
FILED: August 09, 2000 (20000809)
INTL CLASS: H04L-012/28; **G06F-017/50** ; H04L-012/56

ABSTRACT

PROBLEM TO BE SOLVED: To provide a design circuit for supplying the traffic amount of data flowing in from an entrance node and the traffic amount of the data flowing out from an exit node and obtaining a path for service by which communication is arbitrarily possible within the range and a required link capacity.
SOLUTION: An optimization reference preparation means 11 sets an objective function for minimizing link loads and a constraint expression for obtaining the link loads. A route selecting condition preparation means 12 prepares the constraint expression for selecting a route for housing the traffic of the data flowing in. An each user required link capacity calculating condition preparation means 13 prepares the constraint expression for calculating a link band required in each link for each traffic of the data coming in from the entrance node of each user. A link housing condition preparation means 14 prepares the constraint expression for not exceeding a link capacity limit in each link. An optimization means 15 solves mathematical programming problems prepared by the respective means and obtains the path for multi-spot communication service.

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**11/5/2 (Item 2 from file: 347)**
DIALOG(R)File 347:JAPIO
(c) 2003 JPO & JAPIO. All rts. reserv.

07015636 **Image available**
VIRTUAL DESIGN CENTER SYSTEM AND ITS METHOD

PUB. NO.: 2001-243265 [JP 2001243265 A]
PUBLISHED: September 07, 2001 (20010907)
INVENTOR(s): WASHIDA YOSHIHIRO
SUDA TAKESHI
JUFUKU YASUHIRO
APPLICANT(s): TOPPAN PRINTING CO LTD
APPL. NO.: 2000-051545 [JP 200051545]
FILED: February 28, 2000 (20000228)
INTL CLASS: **G06F-017/50** ; **G06F-017/60**

ABSTRACT

PROBLEM TO BE SOLVED: To provide a design and development environment at a low cost, by which coping with the shortening of a life in electronic equipment is flexibly, rapidly and adequately performed, to each designer

regardless of the department and a work place.

SOLUTION: A system for providing the design and development environment of electronic equipment to **Web** clients connected to a **network** is provided with a means for performing **electronic** equipment **design application software** based on a contract in accordance with the request of each user to be performed by using the Web client and displaying the performing result in the Web client and a means for charging to the performing of the software based on the contract.

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**11/5/3 (Item 3 from file: 347)**
DIALOG(R)File 347:JAPIO
(c) 2003 JPO & JAPIO. All rts. reserv.

06848384 **Image available**
RECORDING MEDIUM FOR RECORDING F NET ADAPTABLE ELECTRONIC MAIL PROGRAM

PUB. NO.: 2001-075884 [JP 2001075884 A]
PUBLISHED: March 23, 2001 (20010323)
INVENTOR(s): SAITO TOSHIAKI
SUGA DAISUKE
YOSHIDA TAKEHIRO
KUROSAWA YUJI
YAMAGUCHI AKIICHI
APPLICANT(s): CANON INC
APPL. NO.: 11-249763 [JP 99249763]
FILED: September 03, 1999 (19990903)
INTL CLASS: **G06F-013/00** ; H04N-001/00; H04N-001/32

ABSTRACT

PROBLEM TO BE SOLVED: To provide a recording medium for recording an F net (facsimile communication **network** ) adaptable electronic mail **program** for making it unnecessary to **designate** any **electronic** mail address for operating special distribution instruction at the time of transmitting a multiple address instruction to an F net.
SOLUTION: This is a computer-readable recording medium for recording a program for allowing a computer to execute a procedure for recognizing that electronic mail addresses adaptable to an F net 104 exist in electronic mail addresses designated in an electronic mail address designation column and a procedure for converting the plural electronic mail address corresponding to the F net into telephone number designated multiple address formats when the plural electronic mail addresses corresponding to the F net are inputted, and for transmitting the electronic mails.

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**11/5/4 (Item 4 from file: 347)**
DIALOG(R)File 347:JAPIO
(c) 2003 JPO & JAPIO. All rts. reserv.

06778383 **Image available**
SYSTEM AND METHOD FOR INTEGRATED CIRCUIT DESIGN

PUB. NO.: 2001-005858 [JP 2001005858 A]
PUBLISHED: January 12, 2001 (20010112)
INVENTOR(s): DOLE HARRY
APPLICANT(s): FUJITSU LTD

APPL. NO.: 2000-131709 [JP 2000131709]
FILED: April 28, 2000 (20000428)
PRIORITY: 140528 [US 99140528], US (United States of America), June 20, 1999 (19990620)
478978 [US 2000478978], US (United States of America), January 06, 2000 (20000106)
INTL CLASS: **G06F-017/50** ; H01L-021/82

ABSTRACT

PROBLEM TO BE SOLVED: To provide a system to easily perform recycling or correcting of an IP block when using plural design teams at geographically separated places for executing and testing that design.

SOLUTION: This system is provided with plural computers 2501, 2503 and 2505 equipped with a browser 2507 for displaying a page including an input form, a web server 2507 of at least one methodology server connected through a network 2502 to these computers, provided with a page generator for generating the page including the input form and additionally equipped with a program for responding to the presentation of information from the computer while using the page including the input from and at least one arithmetic processing server 2511 or archive server 2509 connected to the **network** and provided with an electronic design automation tool for executing the **electronic design** automation tool corresponding to a generated request according to a **program** residential on the methodology **server** .

COPYRIGHT: (C)2001,JPO

**11/5/5 (Item 5 from file: 347)**
DIALOG(R)File 347:JAPIO
(c) 2003 JPO & JAPIO. All rts. reserv.

06437183 **Image available**
COMMUNICATION **NETWORK DESIGN CIRCUIT** , ITS METHOD, AND STORAGE MEDIUM RECORDING **PROGRAM** AND READ BY MACHINE

PUB. NO.: 2000-022750 [JP 2000022750 A]
PUBLISHED: January 21, 2000 (20000121)
INVENTOR(s): SAITO HIROYUKI
APPLICANT(s): NEC CORP
APPL. NO.: 10-199619 [JP 98199619]
FILED: June 30, 1998 (19980630)
INTL CLASS: H04L-012/56; **G06F-017/50** ; H04L-012/24; H04L-012/26; H04M-003/00; H04Q-003/00

ABSTRACT

PROBLEM TO BE SOLVED: To design a link capacity and a node capacity of a communication network on the premises that a traffic demand is fluctuated.

SOLUTION: In order to represent fluctuation in a traffic pattern, a demand is given as a random variable. In order to handle a capacity according to the probability distribution as a mathematical programming problem, a satisfaction sale definition equation generating means 102 that defines a satisfaction degree for a request capacity of a demand pair and an expected value lower limit constraint generating means 103 that decides a lower limit of the expected value of the satisfaction degree are provided. Moreover, an optimizing reference generating means 101 that generates an object function to minimize the cost, and a path flow storage constraint

generating means 104, a link allocation constraint generating means 105 and a node allocation constraint generating means 106 that generate constraint equations to obtain a link capacity and a node capacity are provided. In addition, an optimizing means 107 is provided to solve the mathematical programming problems generated by each means above.

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**11/5/6 (Item 6 from file: 347)**
DIALOG(R)File 347:JAPIO
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04206083 **Image available**
DEVICE FOR DESIGNING PRINTED CIRCUIT BOARD

PUB. NO.: 05-197783 [JP 5197783 A]
PUBLISHED: August 06, 1993 (19930806)
INVENTOR(s): HAMANAKA TERUO
APPLICANT(s): MATSUSHITA ELECTRIC IND CO LTD [000582] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 04-008930 [JP 928930]
FILED: January 22, 1992 (19920122)
INTL CLASS: [5] **G06F-015/60** ; H05K-003/00
JAPIO CLASS: 45.4 (INFORMATION PROCESSING -- Computer Applications); 42.1 (ELECTRONICS -- Electronic Components)
JAPIO KEYWORD:R060 (MACHINERY -- Automatic Design)
JOURNAL: Section: P, Section No. 1646, Vol. 17, No. 624, Pg. 72, November 17, 1993 (19931117)

ABSTRACT

PURPOSE: To save power, to shorten a developing period and to improve the accuracy of a design drawing by synchronously advancing circuit diagram design and circuit board design at the time of designing a printed substrate for an electronic apparatus.

CONSTITUTION: In a circuit board designing device constituting a circuit diagram forming device and a circuit board designing device based upon CAD like a **network** through a host computer and capable of executing **circuit** board **design** synchronously with **circuit** diagram **design** by means of **software** for mutually communicating respective device, a circuit diagram is displayed on a display of the circuit diagram forming device and the arrangement state of the parts face of the circuit board or the wiring pattern on the rear face are displayed on a display of the circuit board designing device.

**11/5/7 (Item 1 from file: 350)**
DIALOG(R)File 350:Derwent WPIX
(c) 2003 Thomson Derwent. All rts. reserv.

015232663 **Image available**
WPI Acc No: 2003-293588/200329
XRPX Acc No: N03-233673
**Simulation method for development of microcomputer, involves transmitting hardware simulation command to** HDL **simulator from** software **debugger through communication** network
Patent Assignee: SEIKO EPSON CORP (SHIH )
Number of Countries: 001 Number of Patents: 001
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| JP 2002366602 | A | 20021220 | JP 200262576 | A | 20020307 | 200329 | B |

Priority Applications (No Type Date): JP 2001107942 A 20010406
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| JP 2002366602 | A | | 10 | G06F-017/50 | |

Abstract (Basic): JP 2002366602 A

NOVELTY - A debugger (13) which debugs a software, transmits a command for simulating hardware to hardware desk description language (HDL) simulator (24) through communication network. The HDL simulator inputs received command to hardware bus interface model (31) of hardware simulation model (25) and transmits the simulation result to debugger.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for the following:

(1) Simulation system; and

(2) Simulation program.

USE - For software and hardware development of microcomputer used for printer.

ADVANTAGE - Reduces the software and hardware development period for synchronizing hardware simulation and software debugging.

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of the simulation system. (Drawing includes non-English language text).

Debugger (13)

HDL simulator (24)

Hardware simulation model (25)

Bus interface model (31)

pp; 10 DwgNo 2/6

Title Terms: SIMULATE; METHOD; DEVELOP; MICROCOMPUTER; TRANSMIT; HARDWARE; SIMULATE; COMMAND; SIMULATE; SOFTWARE; THROUGH; COMMUNICATE; NETWORK
Derwent Class: T01
International Patent Class (Main): **G06F-017/50**
International Patent Class (Additional): **G06F-009/455** ; **G06F-011/28**
File Segment: EPI

**11/5/8 (Item 2 from file: 350)**

DIALOG(R)File 350:Derwent WPIX
(c) 2003 Thomson Derwent. All rts. reserv.

015079190 **Image available**
WPI Acc No: 2003-139708/200313
XRPX Acc No: N03-111014

**Digital** circuit design **method used in** networking application , **involves replacing flip flops/RAMs in single phase circuit with TDMA registers/TDMA RAMs**

Patent Assignee: COHEN E T (COHE-I); CISCO TECHNOLOGY INC (CISC-N)
Inventor: COHEN E T
Number of Countries: 001 Number of Patents: 002
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| US 20020175702 | A1 | 20021128 | US 2001826563 | A | 20010404 | 200313 | B |
| US 6556045 | B2 | 20030429 | US 2001826563 | A | 20010404 | 200331 | |

Priority Applications (No Type Date): US 2001826563 A 20010404
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| US 20020175702 | A1 | | 10 | H03K-019/173 | |
| US 6556045 | B2 | | | G06F-007/38 | |

Abstract (Basic): US 20020175702 A1

NOVELTY - The number of copies of a single phase digital circuit, each operating at a lesser rate, than that of the digital circuit is determined, such that the sum of rate of each copy is equal to that of the original circuit. The flip flops/RAMs in the single phase circuit are replaced with TDMA registers/TDMA RAMs, and read, write control signals are provided to each TDMA register/TDMA RAM.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for the following:

(1) Method of converting single phase circuit into TDMA circuit; and

(2) System of converting single phase circuit into TDMA circuit.

USE - For designing multiphase TPMA circuit in networking applications.

ADVANTAGE - The circuit design is easily reconfigurable to run in different modes such as full or partial TDMA or as a single phase. The hardware minimizes the logic area and power required to implement multiple phases of a given function. The hardware is produced from an existing design with purely mechanical changes and thus preserves the existing functionality, and circuit area is efficiently utilized.

DESCRIPTION OF DRAWING(S) - The figure shows a flowchart illustrating conversion of single phase logic circuit to multiphase TDMA circuit.

pp; 10 DwgNo 1/4

Title Terms: DIGITAL; CIRCUIT; DESIGN; METHOD; APPLY; REPLACE; FLIP; RAM; SINGLE; PHASE; CIRCUIT; TDMA; REGISTER; TDMA; RAM

Derwent Class: T01; U11; U14; U21; W01; W02

International Patent Class (Main): **G06F-007/38** ; H03K-019/173

International Patent Class (Additional): H03K-017/16; H03K-019/03

File Segment: EPI

**11/5/9 (Item 3 from file: 350)**

DIALOG(R)File 350:Derwent WPIX

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015072311 **Image available**

WPI Acc No: 2003-132829/200313

XRPX Acc No: N03-105524

**Integrated** circuit design **method e.g. for** application **specific circuit, involves forming another compatible RC** network **and substituting information from high-power cell to low-power cell, when timing error exists**

Patent Assignee: NEC IC MICROCOMPUTER SYSTEMS LTD (NIDE )

Number of Countries: 001 Number of Patents: 001

Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week |
|---|---|---|---|---|---|---|
| JP 2002342400 | A | 20021129 | JP 2001152184 | A | 20010522 | 200313 B |

Priority Applications (No Type Date): JP 2001152184 A 20010522

Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| JP 2002342400 | A | | 19 | G06F-017/50 | |

Abstract (Basic): JP 2002342400 A

NOVELTY - The logical analysis is performed using a high-power cell. The layout of an RC network is formed using a wiring resistor and a capacitor. The delay information is produced by verifying the timing based on the RC network. When timing error exists with respect to delay information, another compatible RC network is formed and the

information from high-power cell is substituted to low-power cell.
USE - For designing large scale integrated circuit (LSI) e.g. application specific integrated circuit (ASIC).
ADVANTAGE - Co-existence of timing conveyance and reduction in electric power are obtained.
DESCRIPTION OF DRAWING(S) - The figure shows a flowchart explaining the LSI design process. (Drawing includes non-English language text).
pp; 19 DwgNo 1/14
Title Terms: INTEGRATE; CIRCUIT; DESIGN; METHOD; APPLY; SPECIFIC; CIRCUIT; FORMING; COMPATIBLE; RC; NETWORK; SUBSTITUTE; INFORMATION; HIGH; POWER; CELL; LOW; POWER; CELL; TIME; ERROR; EXIST
Derwent Class: T01; U11; U13; U21
International Patent Class (Main): **G06F-017/50**
International Patent Class (Additional): H01L-021/82
File Segment: EPI

**11/5/10 (Item 4 from file: 350)**
DIALOG(R)File 350:Derwent WPIX
(c) 2003 Thomson Derwent. All rts. reserv.

015007140 **Image available**
WPI Acc No: 2003-067657/200306
Related WPI Acc No: 2002-528507
XRPX Acc No: N03-052475

**Media content rights management method in internet, involves packaging identified media content in encrypted package and inking media content to usage rules through steganographic identifier**

Patent Assignee: HIATT R S (HIAT-I); LEVY K L (LEVY-I); RHOADS G B (RHOA-I) ; DIGIMARC CORP (DIGI-N)
Inventor: HIATT R S; LEVY K L; RHOADS G B
Number of Countries: 096 Number of Patents: 002
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week |
|---|---|---|---|---|---|---|
| WO 200286803 | A1 | 20021031 | WO 2002US12171 | A | 20020419 | 200306 B |
| US 20020186844 | A1 | 20021212 | US 2000256628 | P | 20001218 | 200306 |
| | | | US 2001285514 | P | 20010420 | |
| | | | US 2001315569 | P | 20010828 | |
| | | | US 2001336209 | P | 20011030 | |
| | | | US 200117679 | A | 20011213 | |
| | | | US 2002126921 | A | 20020418 | |

Priority Applications (No Type Date): US 2002126921 A 20020418; US 2001285514 P 20010420; US 2001315569 P 20010828; US 2000256628 P 20001218 ; US 2001336209 P 20011030; US 200117679 A 20011213
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| WO 200286803 | A1 | E | 3 | G06K-009/00 | |

Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG US UZ VN YU ZA ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZM ZW

| | | | |
|---|---|---|---|
| US 20020186844 | A1 | G06F-017/60 | Provisional application US 2000256628 |
| | | | Provisional application US 2001285514 |
| | | | Provisional application US 2001315569 |
| | | | Provisional application US 2001336209 |
| | | | CIP of application US 200117679 |

Abstract (Basic): WO 200286803 A1

NOVELTY - The media content is identified with a steganographic identifier, by digital watermarking and packaged in an encrypted package. The media content is linked to the usage rules, stored in database server, through the steganographic identifier.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for the following:

(1) Rights management system;
(2) Content distribution chain regulation method;
(3) Distribution regulation method;
(4) Distribution system; and
(5) Content repackaging method.

USE - For performing right management of media content such as audio, video, images, electronic data, biometric information, graphics and **design** , **electronic** document, copyrighted materials of **software** multimedia content transmitted through **internet** , extranet, **web** site, **intranet** , **LAN** , **WAN** , wireless **network** or file transfer transactions.

ADVANTAGE - By linking media content with the usage rules, the copy protection information is allowed to be over-ridden, thereby enabling the sale or distribution of content to end-users and enabling the content owners to be properly paid and users to share content instead of merely prohibiting use of the content and harming the security of the DRM system.

DESCRIPTION OF DRAWING(S) - The figure shows the flowchart illustrating the content management.

pp; 3 DwgNo 1/9

Title Terms: MEDIUM; CONTENT; MANAGEMENT; METHOD; PACKAGE; IDENTIFY; MEDIUM ; CONTENT; ENCRYPTION; PACKAGE; INK; MEDIUM; CONTENT; RULE; THROUGH; IDENTIFY

Derwent Class: T01; W01

International Patent Class (Main): **G06F-017/60** ; G06K-009/00

International Patent Class (Additional): **G06F-017/30**

File Segment: EPI

**11/5/11 (Item 5 from file: 350)**

DIALOG(R)File 350:Derwent WPIX

(c) 2003 Thomson Derwent. All rts. reserv.

014968912 **Image available**

WPI Acc No: 2003-029426/200302

XRPX Acc No: N03-023257

**Integrated** circuit design **system has** application **database that is accessed by user terminals connected to** server **through graphical user interface to perform processes to design integrated circuit**

Patent Assignee: COURTRIGHT D A (COUR-I); JONES D M (JONE-I); KNOWLES J B (KNOW-I); LEV L A (LEVL-I)

Inventor: COURTRIGHT D A; JONES D M; KNOWLES J B; LEV L A

Number of Countries: 001 Number of Patents: 001

Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| US 20020144212 | A1 | 20021003 | US 2001818946 | A | 20010328 | 200302 | B |

Priority Applications (No Type Date): US 2001818946 A 20010328

Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| US 20020144212 | A1 | | 18 | G06F-017/50 | |

Abstract (Basic): US 20020144212 A1

NOVELTY - An application database stores information about several

users and reference design for integrated circuits (ICs). Several terminals connected to several servers performed various processes such as system architecture exploration, software development, design, verification, synthesis and static timing analysis and auto test pattern generation through graphical user interface by accessing the database to design an IC.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for the following:

(1) Integrated circuit design method; and

(2) Computer program product containing integrated circuit design program.

USE - For designing integrated circuits such as application specific integrated circuit (IC).

ADVANTAGE - Enables the design engineers to avoid the purchase of expensive tools for various phases of IC chip design, that are to be used less frequently, thereby the cost and labor required for designing process is reduced.

DESCRIPTION OF DRAWING(S) - The figure shows the flowchart explaining the overall operation of the IC design process.

pp; 18 DwgNo 2/5

Title Terms: INTEGRATE; CIRCUIT; DESIGN; SYSTEM; APPLY; DATABASE; ACCESS; USER; TERMINAL; CONNECT; SERVE; THROUGH; GRAPHICAL; USER; INTERFACE; PERFORMANCE; PROCESS; DESIGN; INTEGRATE; CIRCUIT

Derwent Class: T01; U11; U13

International Patent Class (Main): **G06F-017/50**

File Segment: EPI

**11/5/12 (Item 6 from file: 350)**

DIALOG(R)File 350:Derwent WPIX

(c) 2003 Thomson Derwent. All rts. reserv.

014951391 **Image available**

WPI Acc No: 2003-011904/200301

**Method for inputting electronic mail accounts in mobile communication terminal**

Patent Assignee: LG ELECTRONICS INC (GLDS )

Inventor: AHN Y H

Number of Countries: 001 Number of Patents: 001

Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| KR 2002049957 | A | 20020626 | KR 200079285 | A | 20001220 | 200301 | B |

Priority Applications (No Type Date): KR 200079285 A 20001220

Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| KR 2002049957 | A | | 1 | G06F-017/00 | |

Abstract (Basic): KR 2002049957 A

NOVELTY - A method for inputting an electronic mail account in a mobile communication terminal is provided to increase the convenience of a user by displaying domain names previously set up in the form of a selection list, and by enabling the user to select and designate an address in case that the user inputs a receiver ID to which an electronic mail is transmitted using a radio Internet service.

DETAILED DESCRIPTION - A subscriber connects to an electronic mail management server capable of providing an electronic mail service through a mobile communication network(S10). In case that the **subscriber** wants to **transmit** an electronic mail to a receiver electronic mail account, the **subscriber** selects and **designates** an **electronic** mail **transmission** mode through a key input unit(S11). A

controller confirms whether the **subscriber** inputs the receiver ID(S12). The receiver ID inputted is transmitted to a mail account generating unit(S13). In case that the subscriber selects and inputs an arbitrary domain name(S14), the mail account generating unit combines a user ID with the domain name and generates a receiver mail account(S15). The controller transmits a data file designated as an attached file to the management server(S16).

pp; 1 DwgNo 1/10

Title Terms: METHOD; INPUT; ELECTRONIC; MAIL; ACCOUNT; MOBILE; COMMUNICATE; TERMINAL

Derwent Class: T01

International Patent Class (Main): **G06F-017/00**

File Segment: EPI

**11/5/13 (Item 7 from file: 350)**

DIALOG(R)File 350:Derwent WPIX

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014934239 **Image available**

WPI Acc No: 2002-754948/200282

XRPX Acc No: N02-594762

Network **list generation system for** designing **LSI** circuit , **inspects appropriate arrangement of I/O** software **macro structure based on stored external** network **data, I/O circuit connection data and I/O software macro specification**

Patent Assignee: NEC CORP (NIDE )

Number of Countries: 001 Number of Patents: 001

Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| JP 2002269164 | A | 20020920 | JP 200166453 | A | 20010309 | 200282 | B |

Priority Applications (No Type Date): JP 200166453 A 20010309

Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| JP 2002269164 | A | | 16 | G06F-017/50 | |

Abstract (Basic): JP 2002269164 A

NOVELTY - The external network information about each integrated circuit and input/output circuit connection information and specification of input/output software macro structure are stored in individual memory units. An inspection unit (21) inspects for appropriate arrangement of input/output software macro structure based on information read from memory units and generates the network list, accordingly.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for network list generation program.

USE - For designing LSI circuits.

ADVANTAGE - The network list obtained enables to assign background area which is efficiently and correctly distributed and also hardware macronization of the source synchronous input/output is made unnecessary.

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of the network list generation system. (Drawing includes non-English language text).

Inspection unit (21)

pp; 16 DwgNo 1/11

Title Terms: NETWORK; LIST; GENERATE; SYSTEM; DESIGN; LSI; CIRCUIT; INSPECT; APPROPRIATE; ARRANGE; SOFTWARE; MACRO; STRUCTURE; BASED; STORAGE; EXTERNAL; NETWORK; DATA; CIRCUIT; CONNECT; DATA; SOFTWARE; MACRO; SPECIFICATION

Derwent Class: T01; U11
International Patent Class (Main): **G06F-017/50**
International Patent Class (Additional): H01L-021/82
File Segment: EPI

**11/5/14 (Item 8 from file: 350)**
DIALOG(R)File 350:Derwent WPIX
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014479122 **Image available**
WPI Acc No: 2002-299825/200234
XRPX Acc No: N02-234823
**Communication network-design circuit has optimizing unit which solves mathematical design problem set up by setting unit, to obtain path for multipoint communication service**
Patent Assignee: NEC CORP (NIDE ); SAITO H (SAIT-I)
Inventor: SAITO H
Number of Countries: 002 Number of Patents: 002
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week |
|---|---|---|---|---|---|---|
| JP 2002057676 | A | 20020222 | JP 2000240546 | A | 20000809 | 200234 B |
| US 20020040287 | A1 | 20020404 | US 2001924054 | A | 20010808 | 200245 |

Priority Applications (No Type Date): JP 2000240546 A 20000809
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| JP 2002057676 | A | | 10 | H04L-012/28 | |
| US 20020040287 | A1 | | | G06F-017/50 | |

Abstract (Basic): JP 2002057676 A
NOVELTY - The setting units (11-14) set a mathematical design problem for multipoint communication service. An optimizing unit (15) solves the mathematical design problem, and obtains the path for the communication service.
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:
(a) Recorded medium storing communication **network design circuit** control **program** ;
(b) Transmitter;
(c) Circuit designing method
USE - Communication network-design circuit.
ADVANTAGE - Enables calculation of required link capability based on operation of optimizing unit.
DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of the communication network-design circuit. (Drawing includes non-English language text).
Setting units (11-14)
Optimizing unit (15)
pp; 10 DwgNo 1/4
Title Terms: COMMUNICATE; NETWORK; DESIGN; CIRCUIT; OPTIMUM; UNIT; SOLVING; MATHEMATICAL; DESIGN; PROBLEM; SET; UP; SET; UNIT; OBTAIN; PATH; MULTIPOINT; COMMUNICATE; SERVICE
Derwent Class: T01; W01
International Patent Class (Main): **G06F-017/50** ; H04L-012/28
International Patent Class (Additional): H04L-012/56
File Segment: EPI

**11/5/15 (Item 9 from file: 350)**

DIALOG(R)File 350:Derwent WPIX
(c) 2003 Thomson Derwent. All rts. reserv.

014469651 **Image available**
WPI Acc No: 2002-290354/200233
**Method and system for designing circuit based on network using ip library**
Patent Assignee: IPEAN (IPEA-N)
Inventor: PARK I H
Number of Countries: 001 Number of Patents: 001
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| KR 2001104400 | A | 20011126 | KR 200159536 | A | 20010926 | 200233 | B |

Priority Applications (No Type Date): KR 200057156 A 20000928
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| KR 2001104400 | A | | 1 | G06F-017/50 | |

Abstract (Basic): KR 2001104400 A

NOVELTY - A method and system for designing a circuit based on a network using an IP library is provided to evaluate reliability of an IP data, protect an IP data from external users, and design a circuit using a virtual IP data.

DETAILED DESCRIPTION - An original IP data(42) including a circuit data is stored in an IP server(40) in order to be used in designing a circuit. A virtual IP data is generated to include an interface information of the original IP data. The virtual IP data, an IP symbol, and an **application** for the **circuit design** which can **design** a **circuit** are provided to a pertinent client(50) through a **network** according to the client's request. A **circuit design** data designed by using the **application** for **circuit design** is received from the client. A circuit operation is simulated by using the original IP data corresponding to the virtual IP data included in the circuit design data. The simulation result data is transmitted to the pertinent client. The network is a wired network or a wireless network. The original IP data and the virtual IP data are written using a hardware description language.

pp; 1 DwgNo 1/10

Title Terms: METHOD; SYSTEM; DESIGN; CIRCUIT; BASED; NETWORK; IP; LIBRARY
Derwent Class: T01
International Patent Class (Main): **G06F-017/50**
File Segment: EPI

**11/5/16 (Item 10 from file: 350)**
DIALOG(R)File 350:Derwent WPIX
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014415815 **Image available**
WPI Acc No: 2002-236518/200229
XRPX Acc No: N02-181837
**Circuit design and simulation method involves modifying selected blocks of previously simulated model and classifying blocks into variant, conditional and invariant blocks**
Patent Assignee: NOVAS SOFTWARE INC (NOVA-N); SPRINGSOFT INC (SPRI-N)
Inventor: HUANG Y; LEE C; LU M; TSAI J
Number of Countries: 001 Number of Patents: 001
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| US 6321363 | B1 | 20011120 | US 99228905 | A | 19990111 | 200229 | B |

Priority Applications (No Type Date): US 99228905 A 19990111
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
US 6321363 B1 12 G06F-017/50

Abstract (Basic): US 6321363 B1
NOVELTY - Blocks of a circuit model are simulated in cycles to produce a dump file data indicating states of block input and output signals. Blocks are modified and classified into variant, conditional and invariant blocks. A modified model is simulated with a determined state of output from each conditional block. The output state is determined either from the dump file or from its behavior during the successive simulation.
USE - For use in computer aided verification tools for circuits in chip level or system integration phase such as **electronic design** automation ( **EDA** ) **software** , firmware and/or associated hardware and **circuit design** verification methodologies associated with workstations and distributed **network** systems, etc.
ADVANTAGE - Improves quality and productivity at chip or system integration level design verifications using previous simulation designs and changes in the design. Enables easy storage and management of different design versions and corresponding simulation results.
DESCRIPTION OF DRAWING(S) - The figure shows the flowchart showing the operational steps for the circuit design and simulation method.
pp; 12 DwgNo 4/5
Title Terms: CIRCUIT; DESIGN; SIMULATE; METHOD; MODIFIED; SELECT; BLOCK; SIMULATE; MODEL; CLASSIFY; BLOCK; VARIANT; CONDITION; INVARIANT; BLOCK
Derwent Class: T01; U11
International Patent Class (Main): **G06F-017/50**
File Segment: EPI

**11/5/17 (Item 11 from file: 350)**
DIALOG(R)File 350:Derwent WPIX
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014413585 **Image available**
WPI Acc No: 2002-234288/200229
Related WPI Acc No: 2001-496455; 2002-082858; 2002-164448; 2002-412546; 2003-126874
**I/o probe method for rapid prototyping and mixed inspection method of the same**
Patent Assignee: YANG S Y (YANG-I)
Inventor: YANG S Y
Number of Countries: 001 Number of Patents: 001
Patent Family:
Patent No Kind Date Applicat No Kind Date Week
KR 2001098444 A 20011108 KR 200119104 A 20010402 200229 B

Priority Applications (No Type Date): KR 200111587 A 20010226; KR 200019740 A 20000411
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
KR 2001098444 A 1 G06F-011/26

Abstract (Basic): KR 2001098444 A
NOVELTY - An I/O(input/output) probe method for rapid prototyping and a mixed inspection method of the same are provided to inspect a design of digital circuit rapidly and accurately by performing an object circuit for design inspection on a prototyping board and

performing an I/O probe through an I/O probe additional circuit.
DETAILED DESCRIPTION - A prototyping board or a PCB(printed circuit board)(44) include a number of RFPD(reusable field programmable device)(12). A **server** computer(20) generates a **programming** pattern which performs an I/O probe to an object **circuit** for **design** inspection by using a prototyping system **software** (32), and includes a simulator(34). A relay module(30) performs an interface between the prototyping board or the PCB(44) and the server computer(20) for the I/O probe.
pp; 1 DwgNo 1/10
Title Terms: PROBE; METHOD; RAPID; MIX; INSPECT; METHOD
Derwent Class: T01
International Patent Class (Main): **G06F-011/26**
File Segment: EPI

**11/5/18 (Item 12 from file: 350)**
DIALOG(R)File 350:Derwent WPIX
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014352456 **Image available**
WPI Acc No: 2002-173157/200223
XRPX Acc No: N02-131559
**Application processing method for electronic catalog system, involves determining charge and license limits of supplier dictionary based on public access judgment and indicating conformity verifying program to supplier**
Patent Assignee: TOSHIBA KK (TOKE ); ITO S (ITOS-I)
Inventor: ITO S
Number of Countries: 029 Number of Patents: 004
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week |
|---|---|---|---|---|---|---|
| EP 1176534 | A1 | 20020130 | EP 2001306363 | A | 20010725 | 200223 B |
| US 20020013741 | A1 | 20020131 | US 2001910848 | A | 20010724 | 200223 |
| JP 2002041697 | A | 20020208 | JP 2000224257 | A | 20000725 | 200227 |
| KR 2002009499 | A | 20020201 | KR 200144770 | A | 20010725 | 200254 |

Priority Applications (No Type Date): JP 2000224257 A 20000725
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| EP 1176534 | A1 | E | 57 | G06F-017/60 | |
| Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR | | | | | |
| US 20020013741 | A1 | | | G06F-017/60 | |
| JP 2002041697 | A | | 36 | G06F-017/60 | |
| KR 2002009499 | A | | | G06F-017/00 | |

Abstract (Basic): EP 1176534 A1
NOVELTY - The public access of supplier dictionary is judged, based on the application data received from supplier. The charge and license limits of dictionary are determined, when public access is permitted. The charge limit is indicated to supplier along with verification program. The conformity level is verified using the program and accordingly supplier is charged.
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:
(a) Computer system for application processing;
(b) Recorded medium storing application execution program
USE - For processing access **applications** of electronic catalog system in computer **network** , for electric/ **electronic** component

**design** .

ADVANTAGE - Charging is performed according to the conformity level, thereby reliability of catalog system and mutual compatibility between supplier and standard dictionaries are improved.

DESCRIPTION OF DRAWING(S) - The figure shows a flowchart indicating procedure performed in charging level generation server.

pp; 57 DwgNo 2/32

Title Terms: APPLY; PROCESS; METHOD; ELECTRONIC; CATALOGUE; SYSTEM; DETERMINE; CHARGE; LICENCE; LIMIT; SUPPLY; DICTIONARY; BASED; PUBLIC; ACCESS; INDICATE; CONFORM; VERIFICATION; PROGRAM; SUPPLY

Derwent Class: T01

International Patent Class (Main): **G06F-017/00** ; **G06F-017/60**

International Patent Class (Additional): **G06F-017/30**

File Segment: EPI

**11/5/19 (Item 13 from file: 350)**

DIALOG(R)File 350:Derwent WPIX

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014343745 **Image available**

WPI Acc No: 2002-164448/200221

Related WPI Acc No: 2001-496455; 2002-082858; 2002-234288; 2002-412546

XRPX Acc No: N02-125536

**I/O probing apparatus using state information exchange with circuit for its design verification; performs I/O probe by using additional circuit for IOP-probe or HDL code for representing behavior of additional circuit**

Patent Assignee: YANG S (YANG-I)

Inventor: YANG S

Number of Countries: 022 Number of Patents: 001

Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| WO 200201354 | A1 | 20020103 | WO 2001KR1092 | A | 20010626 | 200221 | B |

Priority Applications (No Type Date): WO 2000KR670 A 20000626

Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| WO 200201354 | A1 | E | 94 | G06F-009/455 | |

Designated States (National): CN JP US

Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR

Abstract (Basic): WO 200201354 A1

NOVELTY - Input/output probing (IOP) interface module (26) may include interface module (27) and interface cable (28). IOP system **software** is performed in a **server** (20), which has e.g. **HDL** simulator or logic simulator, or a cycle-basis simulator or is connected to other computer having an arbitrary simulator through short-and long-distance network or inter-network.

DETAILED DESCRIPTION - IOP interface module (27) connects a server (20) having IOP system software to an arbitrary hardware board (44), which mounts at least one semiconductor chip (for example, FPGA, CPLD, or ASIC) on which the designed digital circuit is realized.

INDEPENDENT CLAIMS are included for:

(a) a combined verification method of emulation and simulation

(b) an input/output probing method

(c) a semiconductor design verification and test device method based on Internet

USE - In a technology of a design verification using I/O probing apparatus.

ADVANTAGE - Allows rapidly and effectively debug, with 100% perfect

signal visibility, a circuit for its design verification which is realized in at least one semiconductor chip equipped on an arbitrary prototyping board or arbitrary PCB and then emulated. Enables the state information exchange with a circuit for its design verification simulated on an arbitrary simulator in a complete automatic method, for making the alternate high-speed functional verification and accurate timing verification possible so that the performance of very effective verification is possible.

DESCRIPTION OF DRAWING(S) - The drawing illustrates schematically an input/output probing apparatus related to the present invention.

input/output probing interface module (26)
interface module (27)
interface cable (28)
server (20)
pp; 94 DwgNo 1/18

Title Terms: PROBE; APPARATUS; STATE; INFORMATION; EXCHANGE; CIRCUIT; DESIGN; VERIFICATION; PERFORMANCE; PROBE; ADD; CIRCUIT; PROBE; CODE; REPRESENT; BEHAVE; ADD; CIRCUIT
Derwent Class: T01; U21
International Patent Class (Main): **G06F-009/455**
File Segment: EPI

**11/5/20 (Item 14 from file: 350)**
DIALOG(R)File 350:Derwent WPIX
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014148514 **Image available**
WPI Acc No: 2001-632733/200173
XRPX Acc No: N01-472576

**Virtual design center system for designing of e.g. electronic devices, performs billing for usage of design software based on contract by which software is obtained from network**

Patent Assignee: TOPPAN PRINTING CO LTD (TOPP )
Number of Countries: 001 Number of Patents: 001
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| JP 2001243265 | A | 20010907 | JP 200051545 | A | 20000228 | 200173 | B |

Priority Applications (No Type Date): JP 200051545 A 20000228
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| JP 2001243265 | A | | 11 | G06F-017/50 | |

Abstract (Basic): JP 2001243265 A

NOVELTY - **Electronic** device **design** is performed by a **web** client using **application software** obtained from a **network** based on a contract. Billing for usage of the software for design is done based on the contract.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a virtual design method.

USE - For providing virtual designing environment of electronic devices e.g. portable telephone, computer, etc., to web client through network.

ADVANTAGE - Software usage fee can be setup reasonably based on demand from web client. Several designers can access the software quickly and accurately.

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of the virtual design center system. (Drawing includes non-English language text).

pp; 11 DwgNo 1/6

Title Terms: VIRTUAL; DESIGN; SYSTEM; DESIGN; ELECTRONIC; DEVICE; PERFORMANCE; BILL; DESIGN; SOFTWARE; BASED; CONTRACT; SOFTWARE; OBTAIN; NETWORK
Derwent Class: T01
International Patent Class (Main): **G06F-017/50**
International Patent Class (Additional): **G06F-017/60**
File Segment: EPI

**11/5/21 (Item 15 from file: 350)**
DIALOG(R)File 350:Derwent WPIX
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013662538 **Image available**
WPI Acc No: 2001-146750/200115
XRPX Acc No: N01-107449
**Business-to-business** application **service provider for** electronic design **automation, has** subscription **controller to** bill **the designer for down loading back a simulated and verified derivative of** electronic design
Patent Assignee: GET2CHIP (GETW-N)
Inventor: BRAUNE B; FERNANDES P; FRANK E; KNAPP D; SCHMIDT H
Number of Countries: 088 Number of Patents: 006
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| WO 200072185 | A2 | 20001130 | WO 2000US14617 | A | 20000526 | 200115 | B |
| AU 200051671 | A | 20001212 | AU 200051671 | A | 20000526 | 200115 | |
| US 6470486 | B1 | 20021022 | US 99136127 | P | 19990526 | 200273 | |
| | | | US 2000574693 | A | 20000517 | | |
| EP 1248989 | A2 | 20021016 | EP 2000936347 | A | 20000526 | 200276 | |
| | | | WO 2000US14617 | A | 20000526 | | |
| US 6516453 | B1 | 20030204 | US 99135902 | P | 19990526 | 200313 | |
| | | | US 2000574572 | A | 20000517 | | |
| JP 2003500745 | W | 20030107 | JP 2000620508 | A | 20000526 | 200314 | |
| | | | WO 2000US14617 | A | 20000526 | | |

Priority Applications (No Type Date): US 2000579825 A 20000525; US 99135902 P 19990526; US 99136126 P 19990526; US 99136127 P 19990526; US 2000574572 A 20000517; US 2000574693 A 20000517; US 2000577426 A 20000522
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| WO 200072185 | A2 | E | 48 | G06F-017/00 | |
| Designated States (National): AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG UZ VN YU ZA ZW | | | | | |
| Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TZ UG ZW | | | | | |
| AU 200051671 | A | | | G06F-017/00 | Based on patent WO 200072185 |
| US 6470486 | B1 | | | G06F-017/50 | Provisional application US 99136127 |
| EP 1248989 | A2 | E | | G06F-017/00 | Based on patent WO 200072185 |
| Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI | | | | | |
| US 6516453 | B1 | | | G06F-017/50 | Provisional application US 99135902 |
| JP 2003500745 | W | | 66 | G06F-017/50 | Based on patent WO 200072185 |

Abstract (Basic): WO 200072185 A2

NOVELTY - The business-to-business **application** service provider (104) comprises an **internet website** with access to at least over designer able to **upload electronic designs** in **hardware description** language ( **HDL** ). An **EDA** -on-demand solution hosted on

the **website** , provides front end **electronic design** automation tool. The **EDA** solution are charged by **pay** -per- **use** fee to create unique intellectual property.

USE - For **electronic design** automation of ASICs used in mobile communication system, **networking** equipment, DVD players etc.

ADVANTAGE - The intellectual property created can be re-used, sold, shared, exchanged and otherwise distributed efficiently and easily from a central for profit clearing house because it is ready to be placed and routed by a back end **EDA** tool.

DESCRIPTION OF DRAWING(S) - The figure shows a block diagram of business-to-business service provider.

Business-to-business **application** service provider (104)

pp; 48 DwgNo 1/20

Title Terms: BUSINESS; BUSINESS; APPLY; SERVICE; ELECTRONIC; DESIGN; AUTOMATIC; **SUBSCRIBER** ; CONTROL; **BILL** ; DESIGN; DOWN; LOAD; BACK; SIMULATE; VERIFICATION; DERIVATIVE; ELECTRONIC; DESIGN

Derwent Class: T01; T05

International Patent Class (Main): **G06F-017/00** ; **G06F-017/50**

International Patent Class (Additional): **G06F-017/60** ; H01L-021/82

File Segment: EPI

**11/5/22 (Item 16 from file: 350)**

DIALOG(R)File 350:Derwent WPIX

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013662440 **Image available**

WPI Acc No: 2001-146652/200115

XRPX Acc No: N01-107357

**Ordering and distribution of electronic books to** subscriber , **involves** sending **authorization signal providing access to books designated by associated order, to terminal of telecommunication system**

Patent Assignee: DISCOVERY COMMUNICATIONS INC (DISC-N)

Inventor: ASMUSSEN M L; HENDRICKS J S; MCCOSKEY J S

Number of Countries: 090 Number of Patents: 004

Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| WO 200062229 | A2 | 20001019 | WO 2000US9542 | A | 20000411 | 200115 | B |
| AU 200043375 | A | 20001114 | AU 200043375 | A | 20000411 | 200115 | |
| EP 1171827 | A2 | 20020116 | EP 2000923210 | A | 20000411 | 200207 | |
| | | | WO 2000US9542 | A | 20000411 | | |
| JP 2002541595 | W | 20021203 | JP 2000611223 | A | 20000411 | 200309 | |
| | | | WO 2000US9542 | A | 20000411 | | |

Priority Applications (No Type Date): US 99289956 A 19990413

Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| WO 200062229 | A2 | E | 141 | G06F-017/60 | |
| | Designated States (National): AE AL AM AT AU AZ BA BB BG BR BY CA CH CN CR CU CZ DE DK DM EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW | | | | |
| | Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW NL OA PT SD SE SL SZ TZ UG ZW | | | | |
| AU 200043375 | A | | | G06F-017/60 | Based on patent WO 200062229 |
| EP 1171827 | A2 | E | | G06F-015/02 | Based on patent WO 200062229 |
| | Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI | | | | |
| JP 2002541595 | W | | 150 | G06F-017/60 | Based on patent WO 200062229 |

Abstract (Basic): WO 200062229 A2

NOVELTY - Electronic book data is provided to terminals in electronic book distribution **network** . The electronic book data is displayed as a menu. An electronic book order that designates one or more electronic books for delivery to terminal, is received. An authorization signal that provides access to one or more **designated electronic** books, is **sent** to terminal and electronic books are distributed.

DETAILED DESCRIPTION - The electronic book order includes unique terminal identification. One or more electronic books are packages as a part of multiplex data stream and the multiplex data stream is broadcasted. The electronic order is received at remote location. A billing order is generated based on electronic book order.

USE - For delivery of electronic books to public libraries, book stores, schools, and other customers and for distribution of electronic text and graphics to **subscribers** .

ADVANTAGE - Eliminates distribution of physical object like paper book or computer memory device from any book or text distribution system. Enables to provide continuous distribution of electronic book data including requested electronic books from **subscriber** , electronic books to be broadcast to all **subscribers** , updated menu contents and updated advertising.

DESCRIPTION OF DRAWING(S) - The figure shows the digital television **program** environment.

pp; 141 DwgNo 19/34

Title Terms: ORDER; DISTRIBUTE; ELECTRONIC; BOOK; **SUBSCRIBER** ; **SEND** ; AUTHORISE; SIGNAL; ACCESS; BOOK; DESIGNATED; ASSOCIATE; ORDER; TERMINAL; TELECOMMUNICATION; SYSTEM

Derwent Class: T01; W01; W02

International Patent Class (Main): **G06F-015/02** ; **G06F-017/60**

International Patent Class (Additional): **G06F-017/21** ; **G06F-017/22** ; **G06F-017/30** ; H04N-005/44; H04N-005/76; H04N-007/173

File Segment: EPI

**11/5/23 (Item 17 from file: 350)**

DIALOG(R)File 350:Derwent WPIX

(c) 2003 Thomson Derwent. All rts. reserv.

013560441 **Image available**

WPI Acc No: 2001-044648/200106

XRPX Acc No: N01-033753

**Recording medium for internet based circuit designing, has different recording areas for storing different circuit information with relevant tags**

Patent Assignee: MATSUSHITA DENKI SANGYO KK (MATU )

Number of Countries: 001 Number of Patents: 001

Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| JP 2000305970 | A | 20001102 | JP 99114473 | A | 19990422 | 200106 | B |

Priority Applications (No Type Date): JP 99114473 A 19990422

Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| JP 2000305970 | A | | 10 | G06F-017/50 | |

Abstract (Basic): JP 2000305970 A

NOVELTY - The functional specification description and production information of each circuit, operation information, design procedure description and display information for each circuit are collected.

Different description information are recorded in different areas with separate start and completion tags.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

(a) circuit design procedure;

(b) design data forwarding system

USE - For storing Verilog-high definition language ( **HDL** ) **program** used for **designing** LSI **circuits** using **internet** .

ADVANTAGE - Since different descriptions are recorded in different areas along with tags quick retrieval and transfer of data is enabled.

DESCRIPTION OF DRAWING(S) - The figure shows the design data forwarding system.

pp; 10 DwgNo 1/12

Title Terms: RECORD; MEDIUM; BASED; CIRCUIT; DESIGN; RECORD; AREA; STORAGE; CIRCUIT; INFORMATION; RELEVANT; TAG

Derwent Class: T01; U11

International Patent Class (Main): **G06F-017/50**

International Patent Class (Additional): H01L-021/82

File Segment: EPI

**11/5/24 (Item 18 from file: 350)**

DIALOG(R)File 350:Derwent WPIX

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013121046 **Image available**

WPI Acc No: 2000-292917/200025

Related WPI Acc No: 1999-032984; 2000-373819

XRPX Acc No: N00-219670

**Prototyping system has** server **computer which partitions** designed circuit **into partial circuits and allocates them to respective reusable field** programmable **device of prototyping engine**

Patent Assignee: YANG S (YANG-I); YANG S Y (YANG-I); YANG Y (YANG-I)

Inventor: YANG S; YANG S Y; YANG Y

Number of Countries: 021 Number of Patents: 004

Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| WO 200017912 | A2 | 20000330 | WO 99KR571 | A | 19990920 | 200025 | B |
| EP 1055254 | A2 | 20001129 | EP 99944913 | A | 19990920 | 200063 | |
| | | | WO 99KR571 | A | 19990920 | | |
| KR 2000020291 | A | 20000415 | KR 9838834 | A | 19980919 | 200104 | |
| US 6263484 | B1 | 20010717 | US 98164758 | A | 19981001 | 200148 | |

Priority Applications (No Type Date): KR 9838834 A 19980919; KR 9750810 A 19971001

Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| WO 200017912 | A2 | E | 85 | H01L-000/00 | |
| Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE | | | | | |
| EP 1055254 | A2 | E | | H01L-021/00 | Based on patent WO 200017912 |
| Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE | | | | | |
| KR 2000020291 | A | | | G06F-017/00 | |
| US 6263484 | B1 | | | G06F-017/50 | |

Abstract (Basic): WO 200017912 A2

NOVELTY - A server computer (40) partitioning a predetermined designed circuit to be verified, into several partial circuits and allocates them to respective reusable field programmable device (RFPD) (10) of a prototyping engine (44). The interface module (42) acts as an

interface between server computer and prototype engine.

DETAILED DESCRIPTION - The prototyping engine comprises several component devices such as reusable field programmable device (RFPD) connected by communication ports. Each RFPD comprises an additional circuit for R-communication which transmits signal values among component devices using communication ports. An INDEPENDENT CLAIM is also included for prototyping method.

USE - For verifying designed system level digital circuits.

ADVANTAGE - Enables probing of signal lines in designed system level digital circuits in real time and an automated operating technique, hence improving verification efficiency of digital circuits. The RFPD has high integration degree, hence capability of prototyping engine is increased.

DESCRIPTION OF DRAWING(S) - The figure shows the schematic diagram of prototyping system.

reusable field programmable device (10)
server computer (40)
interface module (42)
prototyping engine (44)
pp; 85 DwgNo 1/38

Title Terms: SYSTEM; SERVE; COMPUTER; PARTITION; DESIGN; CIRCUIT; CIRCUIT; ALLOCATE; RESPECTIVE; REUSE; FIELD; PROGRAM; DEVICE; ENGINE
Derwent Class: T01; U11; U13
International Patent Class (Main): **G06F-017/00 ; G06F-017/50 ;** H01L-000/00; H01L-021/00
International Patent Class (Additional): **G06F-017/00 ;** AFH0-1L000/00; AF-H01L021/00
File Segment: EPI

**11/5/25 (Item 19 from file: 350)**
DIALOG(R)File 350:Derwent WPIX
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012965071 **Image available**
WPI Acc No: 2000-136922/200012
Related WPI Acc No: 2001-023234
XRPX Acc No: N00-102376

**Thrust pulses controlling device for pulsed rocket motor tactical missile**

Patent Assignee: RAYTHEON CO (RAYT )
Inventor: BIGGERS J E; FINN K P; SCHWARTZ H H
Number of Countries: 025 Number of Patents: 002
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| WO 9966418 | A2 | 19991223 | WO 99US227 | A | 19990106 | 200012 | B |
| AU 9962371 | A | 20000105 | AU 9962371 | A | 19990106 | 200024 | |

Priority Applications (No Type Date): US 984993 A 19980109
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| WO 9966418 | A2 | E | 21 | G06F-015/00 | |

Designated States (National): AU CA IL JP KR NO TR
Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE

| | | | | |
|---|---|---|---|---|
| AU 9962371 | A | | G06F-015/00 | Based on patent WO 9966418 |

Abstract (Basic): WO 9966418 A2

NOVELTY - The missile includes a fuselage with pulse propulsion system. The pulsed propulsion system has N-pulse motor system which produces successive thrust pulses in response to pulse trigger commands provided to pulsed propulsion output. An on-board neural network

controller controls at least one of the thrust pulses at optimal time in dependence on a set of input conditions, by providing pulse trigger commands.

USE - For pulsed rocket motor tactical missile.

ADVANTAGE - The neural network effectively learns the correlation between input and output and thus predicts input-output relationships not previously seen in any training case. The implementation of neural **networks** in **electronic circuit design** tends itself to **applications** in space and weight limited missiles. When implemented in logic device, the neural **network** relation between multiple input expressions reduce to compact and efficient form.

DESCRIPTION OF DRAWING(S) - The figure shows the graphical representation of neural network controller.

pp; 21 DwgNo 2/6

Title Terms: THRUST; PULSE; CONTROL; DEVICE; PULSE; ROCKET; MOTOR; TACTICAL ; MISSILE

Derwent Class: T01; T06; W07

International Patent Class (Main): **G06F-015/00**

File Segment: EPI

**11/5/26 (Item 20 from file: 350)**

DIALOG(R)File 350:Derwent WPIX

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012872811 **Image available**

WPI Acc No: 2000-044644/200004

XRPX Acc No: N00-034224

**Electric circuit design apparatus for use in computer, radio apparatus, etc - has memory to store information about network and component library with signal line name generator**

Patent Assignee: TOSHIBA KK (TOKE )

Number of Countries: 001 Number of Patents: 001

Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| JP 11306209 | A | 19991105 | JP 98107197 | A | 19980417 | 200004 | B |

Priority Applications (No Type Date): JP 98107197 A 19980417

Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| JP 11306209 | A | | 9 | G06F-017/50 | |

Abstract (Basic): JP 11306209 A

NOVELTY - The apparatus has a memory (10) to store the information about the network. A signal line name generator (30) is provided to the component library (12) which adds at least a character row to the **network** . DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for electric **circuit designing program** .

USE - For designing electric circuit in computer, radio apparatus, etc for confirmation and correction of existence of unsuitable wiring in printed circuit board designing.

ADVANTAGE - Since the apparatus has signal line name genertor, the burden of the designer is reduced. The work hour for circuit design is reduced. DESCRIPTION OF DRAWING(S) - The figure shows block diagram of electric circuit design apparatus. (10) Memory; (12) Component library; (30) Signal line name generator.

Dwg.1/6

Title Terms: ELECTRIC; CIRCUIT; DESIGN; APPARATUS; COMPUTER; RADIO; APPARATUS; MEMORY; STORAGE; INFORMATION; NETWORK; COMPONENT; LIBRARY; SIGNAL; LINE; NAME; GENERATOR

Derwent Class: T01; U11
International Patent Class (Main): **G06F-017/50**
File Segment: EPI

**11/5/27 (Item 21 from file: 350)**
DIALOG(R)File 350:Derwent WPIX
(c) 2003 Thomson Derwent. All rts. reserv.

012694589 **Image available**
WPI Acc No: 1999-500698/199942
XRPX Acc No: N99-373855

**Communication network-design circuit - converts capacity constraint equations and objective function which minimizes cost about link and node, to deterministic program problem which is solved to determine capacity of link and node**

Patent Assignee: NEC CORP (NIDE )
Inventor: SAITO H
Number of Countries: 002 Number of Patents: 003
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| JP 11215124 | A | 19990806 | JP 989982 | A | 19980122 | 199942 | B |
| US 6404744 | B1 | 20020611 | US 99235733 | A | 19990122 | 200246 | N |
| JP 3329254 | B2 | 20020930 | JP 989982 | A | 19980122 | 200271 | |

Priority Applications (No Type Date): JP 989982 A 19980122; US 99235733 A 19990122
Patent Details:

| Patent No | Kind | Lan | Pg | Main IPC | Filing Notes |
|---|---|---|---|---|---|
| JP 11215124 | A | | 29 | H04L-012/00 | |
| US 6404744 | B1 | | | H04L-012/28 | |
| JP 3329254 | B2 | | 29 | H04L-012/56 | Previous Publ. patent JP 11215124 |

Abstract (Basic): JP 11215124 A

NOVELTY - A deterministic program problem converter (5) changes the constraint equations and an objective function for minimizing cost about the link and node, to a deterministic program problem. The capacity of the link and node is determined by an optimization device (6) by solving the deterministic program problem. DETAILED DESCRIPTION - The constraint equations for accommodating the demand capacity among arbitrary nodes in a path, for accommodating the capacity assigned to the path in a link, and for accommodating the capacity assigned to a path in the node, are produced.INDEPENDENT CLAIMS are also included for the following:a communication network-design method; and a recording medium for the control program.

USE - For designing communication network consisting of link which connects nodes.

ADVANTAGE - Communication traffic can be accommodated even when demand pattern changes. DESCRIPTION OF DRAWING(S) - The figure shows a block diagram of the communication **network - design circuit** . (5) Deterministic **program** problem converter; (6) Optimization device.

Dwg.1/10

Title Terms: COMMUNICATE; NETWORK; DESIGN; CIRCUIT; CONVERT; CAPACITY; CONSTRAIN; EQUATE; OBJECTIVE; FUNCTION; MINIMISE; COST; LINK; NODE; PROGRAM; PROBLEM; SOLVING; DETERMINE; CAPACITY; LINK; NODE
Derwent Class: T01; W01
International Patent Class (Main): H04L-012/00; H04L-012/28; H04L-012/56
International Patent Class (Additional): **G06F-013/00** ; **G06F-017/50** ; H04M-003/00
File Segment: EPI

**11/5/28 (Item 22 from file: 350)**
DIALOG(R)File 350:Derwent WPIX
(c) 2003 Thomson Derwent. All rts. reserv.

002086635
WPI Acc No: 1979-A6522B/197904
**Access logic circuit for telephone subscriber terminal - sends data to central computer and receives commands from it**
Patent Assignee: THOMSON CSF (CSFC )
Number of Countries: 007 Number of Patents: 007
Patent Family:

| Patent No | Kind | Date | Applicat No | Kind | Date | Week | |
|---|---|---|---|---|---|---|---|
| BE 870354 | A | 19790102 | | | | 197904 | B |
| DE 2839174 | A | 19790315 | | | | 197912 | |
| NL 7809173 | A | 19790313 | | | | 197913 | |
| SE 7809363 | A | 19790402 | | | | 197916 | |
| GB 2007464 | A | 19790516 | | | | 197920 | |
| FR 2402977 | A | 19790511 | | | | 197924 | |
| IT 1105797 | B | 19851104 | | | | 198714 | |

Priority Applications (No Type Date): FR 7727311 A 19770909

Abstract (Basic): BE 870354 A
The access logic **circuit** , is **designed** for use in a telephone **subscriber** terminal. It **sends** information signals between a central computer and a group of **subscriber** circuits managed by the computer. The information comprises commands emitted by the computer and data sent to it.
A first group of registers records the data signals which a second group records the commands. The data signals and commands travel via separate buses or highways. The marker signal is retained by a further register
Title Terms: ACCESS; LOGIC; CIRCUIT; TELEPHONE; SUBSCRIBER; TERMINAL; SEND; DATA; CENTRAL; COMPUTER; RECEIVE; COMMAND
Derwent Class: T01; U21; U22; W01
International Patent Class (Additional): **G06F-013/00** ; H03K-000/00; H04M-003/00; H04Q-003/44
File Segment: EPI